

## Software Functional Overview

### 3.1 Overview

The A985 is an IBM PC/AT compatible Notebook PC which supports the Intel uFCPGA Socket Pentium IV processor family. The following are the major features that A985 supports.

- § Microsoft PC99 logo and WinXP logo approval.
- § 14.1" XGA TFT panel support.
- § 15" XGA and SXGA+ TFT panel support.
- § APM 1.2 compliance
- § Support ACPI 1.0B (or above).
- § Support PCI 2.1 (or above).
- § Support AGP 2.0.
- § Support USB 1.1.
- § Support SMBIOS 2.2.
- § Support 100 MHz CPU front side bus.
- § Support a proprietary Port Replicator

### 3.2 Summary of the BIOS Specification

Below is the summary of the BIOS software specification:

Controller Chip	Description
<b>BIOS Feature</b>	Microsoft PC99 logo and WinXP logo approval. § Support Boot Block / Crisis Rescue § Support ACPI 1.0B (or above) Spec. § Support PCI 2.1 (or above) Spec. § Support SMBIOS 2.3 Spec § Support AGP 2.0 Spec. § Support Windows 2000 and Windows XP. § Support flash function including both DOS and Windows interface for new BIOS update. § Support 3 Mode FDD. § Support 4 different keyboards on same BIOS. § Support boot from FDD, HDD and CDROM Drive
<b>CPU</b>	Auto detect the CPU type and speed for the Intel Pentium 4 based system
<b>DRAM</b>	Auto sizing and detection. Support PC-266 DDR SDRAM.
<b>Cache</b>	§ Level 2 SRAM auto sizing and detection § Always enable CPU L1 and L2 cache.
<b>Shadow</b>	Always enable VGA and System BIOS shadow

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Controller Chip	Description
<b>Display</b>	<ul style="list-style-type: none"> <li>§ System auto detects LCD or CRT presence on boot and lid closed</li> <li>§ Support Panning while LCD in a display resolution greater than supported</li> <li>§ Support Microsoft Direct 3D</li> <li>§ Support AGP 4x BUS</li> </ul>
<b>Hard Disk</b>	<ul style="list-style-type: none"> <li>§ Enhanced IDE spec.</li> <li>§ Support auto IDE detection.</li> <li>§ Support LBA mode for larger capacity HDD.</li> <li>§ Support Ultra DMA 33/66/100.</li> <li>§ Support Fast PIO mode 1-4 transfer.</li> <li>§ Support 32 bit PIO transfer.</li> <li>§ Support Multi-Sector transfer.</li> <li>§ Support SMART monitoring.</li> </ul>
<b>Multi Boot</b>	Allow the user to select boot from USB FDD, HDD and CD-ROM
<b>Plug and Play</b>	Support PnP Run Time Service and conflict-free allocation of resource during POST
<b>Smart Battery</b>	Support BIOS interface to pass battery information to the application via SMBus.
<b>Keyboard Controller</b>	Support Fn hot keys, two Windows hot keys, built-in Glide Pad and external PS/2 mouse/keyboard
<b>PCMCIA</b>	Compliant with PCMCIA 2.1 specification.
<b>Port Replicator</b>	I/O port replicator duplicates the following ports <ul style="list-style-type: none"> <li>§ Video port</li> <li>§ Printer port</li> <li>§ COM port</li> <li>§ USB Port</li> <li>§ DC In Jack</li> </ul>
<b>Power Management Support</b>	The power management is compliant with ACPI 1.0B / ACPI 2.0 specification and supports the following power state: <ul style="list-style-type: none"> <li>§ C2/C3 – Doze Mode</li> <li>§ S1 – Suspend to RAM (STR) Mode</li> <li>§ S4 – Suspend to Disk (STD) Mode</li> <li>§ S5 – Soft-Off Mode (SOff)</li> </ul>

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## 3.3 Subsystem Software Functions

This section provides introduction on the software functions of the notebook subsystems and BIOS related function.

### 3.3.1 Key Chipset Summary

Following are the main chipsets used in the notebook:

Controller Chip	Vendor	Description
Processor	Intel	Pentium 4 – M Northwood
North Bridge	SIS	SIS 650
South Bridge	SIS	SIS 961
Video Controller	SIS	Embedded in SIS 650
PCMCIA Controller	O2Micro	OZ6912
Supper I/O Controller	SMSC	LPC47N267
Audio Controller	SIS	South Bridge Integrated
Audio Codec	Realtek	ALC 201
Keyboard Controller	ENE	KB38867
PMU Controller	Mitsubishi	PMU08
ROM BIOS	SST	49LF040A
IEEE 1394	Lucent	Fw322
On board LAN	Realtek	8100BL
BlueTooth	SIS	Embedded in SIS 961 USB interface
GPRS Module		Support GSM 900/1800MHZ
Modem	MDC	AC97 Interface

### 3.3.2 System Memory

The system memory consists of SDRAM memory on 64-bit bus and the module size options are 128/256/512MB upward. The BIOS will automatically detect the amount of memory in the system and configure CMOS accordingly during the POST (Power-On Self Test) process. This must be done in a way that requires no user interaction.

Base SO-DIMM DRAM slot (Bank 0 & 1)	Base SO-DIMM DRAM slot (Bank 2 & 3)	Total Size
NIL	128MB	128MB
NIL	256MB	256MB
NIL	512MB	512MB

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128MB	NIL	128MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	NIL	256MB
256MB	128MB	384MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	NIL	512MB
512MB	128MB	640MB
512MB	256MB	768MB
512MB	512MB	1024MB

### 3.3.3 Video

The Video subsystem use share memory of Video memory. The system will support Microsoft direct 3D, Dual display support ,simultaneous display, monitor sense for auto display on boot and VESA Super VGA function call.

### 3.3.4 Supported Video Mode

The following is the display modes supported by the SIS Mobility Video control in LCD only, CRT only, and simultaneous mode. The VGA BIOS will allow mode sets of resolutions greater than the panel size but only show as much mode display as will fit on the panel.

- **Supported Standard VGA Mode**

The VGA BIOS supports the IBM VGA Standard 7-bit VGA modes numbers.

Mode	Pixel Resolution	Colors	Memory
00h/01h	40*25	16	Text
02h/03h	80*25	16	Text
04h/05h	320*200	4	2-bit Planar
06h	640*200	2	1-bit Planar
07h	80*25	Mono	Text
0Dh	320*200	16	4-bit Planar
0Eh	640*200	16	4-bit Planar
0Fh	640*350	Mono	1-bit Planar

Mode	Pixel Resolution	Colors	Memory
10h	640*350	16	4-bit Planar
11h	640*480	2	2-bit Planar
12h	640*480	16	4-bit Planar
13h	320*200	256	8-bit Planar

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Note: All Standard VGA Modes are limited to the standard VGA refresh rates.

- Supported extended video modes**

CRT device will support all listed VESA mode; and other devices such as PANEL & TV may be limited to the mode support due to their characteristics

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VESA Mode	Pixel Resolution	Memory Model	Refresh Rates In (Hz)	Minimum Memory
100h	640 x 400	8-bit Packed	70	2MB
101h	640 x 480	8-bit Packed	60, 72, 75, 85	2MB
102h	800 x 600	4-bit Planar	60, 72, 75, 85, 100	2MB
103h	800 x 600	8-bit Packed	60, 72, 75, 85, 100	2MB
104h	1024 x 768	4-bit Planar	43(I), 60, 70, 75, 85, 100	2MB
105h	1024 x 768	8-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
106h	1280 x 1024	4-bit Planar	43(I), 60, 75, 85	2MB
107h	1280 x 1024	8-bit Packed	43(I), 60, 75, 85	2MB
10Eh	320 x 200	16-bit Packed	70	2MB
10Fh	320 x 200	32-bit Unpacked	70	2MB
111h	640 x 480	16-bit Packed	60, 72, 75, 85	2MB
112h	640 x 480	32-bit Unpacked	60, 72, 75, 85	2MB
114h	800 x 600	16-bit Packed	60, 72, 75, 85, 100	2MB
115h	800 x 600	32-bit Unpacked	60, 72, 75, 85, 100	2MB
117h	1024 x 768	16-bit Packed	43(I), 60, 70, 75, 85, 100	2MB
118h	1028 x 768	32-bit Unpacked	43(I), 60, 70, 75, 85, 100	4MB
11Ah	1280 x 1024	16-bit Packed	43(I), 60, 75, 85	4MB
11Bh	1280 x 1024	32-bit Unpacked	43(I), 60, 75, 85	8MB
11Dh	640 x 400	16-bit Packed	70	2MB
11Eh	640 x 400	32-bit Packed	70	2MB
120h	1600 x 1200	8-bit Packed	48(I), 60, 75, 85	2MB
VESA Mode	Pixel Resolution	Memory Model	Refresh Rates In (Hz)	Minimum Memory
122h	1600 x 1200	16-bit Packed	48(I), 60, 75, 85	4MB
124h	1600 x 1200	32-bit Unpacked	48(I), 60, 75, 85	8MB
12Ah	640 x 480	24-bit Packed	60, 72, 75, 85	2MB

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12Bh	800 x 600	24-bit Packed	60, 72, 75, 85, 100	2MB
12Ch	1024 x 768	24-bit Packed	43(I), 60, 70, 75, 85, 100	4MB
12Dh	1280 x 1024	24-bit Packed	43(I), 60, 75, 85	4MB
12Eh	320 x 200	8-bit Packed	70	2MB
131h	320 x 200	8-bit Packed	72	2MB
133h	320 x 200	16-bit Packed	72	2MB
134h	320 x 200	32-bit Packed	72	2MB
13Bh*	1400 x 1050	8-bit Packed	60, 75	2MB
13Ch*	1400 x 1050	16-bit Packed	60, 75	4MB
13Eh*	1400 x 1050	32-bitUnpacked	60, 75	8MB
141h	400 x 300	8-bit Packed	72	2MB
143h	400 x 300	16-bit Packed	72	2MB
144h	400 x 300	32-bitUnpacked	72	2MB
151h	512 x 384	8-bit Packed	70	2MB
153h	512 x 384	16-bit Packed	70	2MB
154h	512 x 384	32-bitUnpacked	70	2MB
171h	720 x 480	8-bit Packed	75	2MB
173h	720 x 480	16-bit Packed	75	2MB
174h	720 x 480	24-bit Packed	75	2MB
175h	720 x 480	32-bitUnpacked	75	2MB
176h	720 x 576	8-bit Packed	75	2MB
178h	720 x 576	16-bit Packed	75	2MB
179h	720 x 576	24-bit Packed	75	2MB
17Ah	720 x 576	32-bitUnpacked	75	2MB

Note: “\*” The modes may not be available. Their availability should be determined by VESA function calls.

### I Panel Type Initialization

The VGA BIOS will issue INT 15h function call during POST. This function call allows the system BIOS to specify the panel type to the VGA BIOS. The system BIOS should get the panel type from GPI pins before the VGA chip initialized, and pass this information to VGA BIOS through INT 15 Function code.

#### – LCD Panel ID pin Definition:

GPI[45]	GPI[46]	GPI[10]	GPI[22]	Panel Type
0	0	0	0	
0	0	0	1	

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0	0	1	0	
0	0	1	1	LP150U1 (LG)
0	1	0	0	
0	1	0	1	
0	1	1	0	B141PN01 (AU)
0	1	1	1	HSD141PX11-A (Hannstar)
1	0	0	0	CPTCLAA141XF 01 (CPT)
1	0	0	1	LTN141X8-L04 (Samsung)
1	0	1	0	B141XN04V2 (AU)
1	0	1	1	B150XN01(AU)
1	1	0	0	LTN150U1-L02 (Samsung)
1	1	0	1	LTN150P3-L04 (Samsung)
1	1	1	0	B150PN01 (AU)
1	1	1	1	HSD150PK12-A (Hannstar)

### 3.3.5 Enhanced IDE

The system BIOS supports 4 IDE devices on two controllers up to 30 GB capacity. The BIOS support Ultra DMA 33/66/100 and also supports automatic configuration of drives using both the LBA and CHS large drive remapping method. In addition to supporting standard drives through an auto-configuration process that does NOT require user involvement or confirmation. The system should automatically do this at POST time in a way that is transparent to the user. If a drive is connected to the bus, the drive should be automatically recognized, configured and available for use under MS-DOS 6.2x.

### 3.3.6 Audio

The audio subsystem will support the requirements identified by the AC'97 specification. Both software and hardware will control the volume level for the internal audio subsystem. In addition to the volume control, the user will be able to mute the sound to completely cut off the volume using both software and hardware.

### 3.3.6 Super I/O

This controller contains 16550A or FIFO Enabled UART, ECP/EPP/Uni-directional Parallel Port meeting the 1284 specification, and an Infrared port.

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### 3.3.7 PCMCIA

The PCMCIA controller chip of the notebook provides the following features:

- Support for only single CardBus slot (two type II stacked)
- Individually accessed, dual-buffer implementation
- Support for 3.3v, 5v and 12v (flash programming) cards

### 3.3.8 LED Indicator

The table below lists down the functions of the Status LED indicator:

Indicator	Function Description
<b>PowerButton LED</b>	Those LEDs indicate user the button's location in the dark.
<b>IDE accessing LED</b>	This LED will turn on while accessing the IDE Device.
<b>FDD accessing LED</b>	This LED will turn on while accessing the FDD Device.
<b>Battery Charging LED</b>	Turn on (Amber) – Battery is under charging mode Turn off – Battery full charged or no battery
<b>CapsLock LED</b>	This LED will turn on when the function of CapsLock is active.
<b>ScrollLock LED</b>	This LED will turn on when the function of ScrollLock is active.
<b>NumLock LED</b>	This LED will turn on when the function of NumLock is active.
<b>Power Status LED</b>	This LED will turn on whe system is powered on, and blinking when system is Entered into standby mode.

**i** - There LEDs will be turned off during Suspend mode.

**v**:

Power Source	Lid Status	System Status	
		On	Off
AC adapter	Open	Off	Always On
	Close	Off	Off
Battery only	Open	Off	On for 4 secs and then Off
	Close	Off	Off

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### 3.3.9 Hot Keys Definition

All Hot keys must be active at all times under all operation systems.

#### Hot Keys by Internal Keyboard

Hot Key	Function	Handler
Fn + F3	Toggle Display (LCD/CRT/LCD&CRT)	BIOS Handler
Fn + F4	System entered into standby mode	BIOS Handler
Fn + F6	System Speaker On/Off	BIOS Handler



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Fn + F8	Brightness Increase	Controlled by PMU08
Fn + F9	Brightness Decrease	Controlled by PMU08
Internet Button	Internet Function Key	Controlled by Driver
Mail Button	Mail Function Key	Controlled by Driver

### Port Replicator

The Port Bar duplicates the following ports from the Notebook:

- § CRT port
- § Serial port
- § Printer port
- § Two USB Ports
- § DC In Jack

The Port replicator can just support the cold insertion but not hot insertion. While hot insertion, the system is not guarantee that functionality.

### 3.3.10 Plug & Play

The BIOS supports the Plug and Play Specification 1.0A. (Include ESCD) This section describes the device management. The system board devices and its resources are as follows:

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Device	Connect Type	Resources			
		I/O	IRQ	DMA	Memory
DMA Controller	Static	00~0F, 81~8F	-	DMA4	-
Interrupt Controller	Static	20~21, A0~A1	IRQ2	-	-
System Timer	Static	40~43	IRQ0	-	-
RTC	Static	70~71	IRQ8	-	-
ISA Bus	Static	-	-	-	-
System Speaker	Static	61	-	-	-
System Board	Static	-	-	-	E0000~FFFFFF
PnP Mother Board	Static	80	-	-	-
Keyboard Controller	Static	60, 64	IRQ1	-	-
PMU08 Controller	Static	68, 6C	-	-	-
Math Coprocessor	Static	F0~FF	IRQ13	-	-
PS/2 Mouse	Enable / Disable Static	-	IRQ12	-	-
Video Controller	Static	3B0~3BB, 3C0~3DF	IRQ5	-	A0000~BFFFF, C0000~CFFFF
Serial Port	Static	3F8~3FF	IRQ4	-	-
ECP, Parallel port	Dynamic	378~37F, 778~77F	IRQ7	DMA1	-
FDC	Dynamic	3F0~3F5, 3F7	IRQ6	DMA2	-
Dual IDE Controller	Static	170~177, 1F0~1F7, 3F6	IRQ14, 15	-	-
CardBus Controller	Static	3E0~3E1	IRQ11	-	-
Audio chip	Dynamic	220~22F, 300~301, 388~38B	IRQ5	DMA3	-
IEEE1394	Dynamic		IRQ11		
Modem	Dynamic	3E8~3EF	IRQ10	-	-
LAN	Dynamic	1080~10FF	IRQ10	-	-
SIR	Enable / Disable	158~15F, 2F8- 2FF	IRQ3	-	-
USB Host Controller	Dynamic	EF80~EF9F	IRQ5	-	-

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- **PCI Device**

The table below summarizes the PCI IDSEL Pin Allocation:

IDSEL Pin	PCI	Device	
	Device Number	Function Number	Device Name
AD11	Device 00	Function 0	SIS650 - Host to PCI bridge
AD17	Device 06	Function 0	LAN / Modem
		Function 0	SIS961 - PCI to ISA bridge
		Function 1	SIS961 - IDE interface
		Function 2	SIS961 - USB Port 0-1 interface
AD18	Device 07	Function 3	SIS961 - USB Port 2-3 interface
		Function 4	SIS961 - PMU and SMBus interface
		Function 5	SIS961 - AC97 Audio interface
		Function 6	SIS961 - AC97 Modem interface
AD20	Device 09	Function 0	LAN/Modem
AD23	Device 0C	Function 0	OZ6912 - Card Bus Socket A
		Function 1	OZ6912 - Card Bus Socket B
AD24	Device 0D	Function 0	IEEE1394

The table below summarizes the INT Pin Allocation:

INT Pin	PCI Device
INTA	CardBus/1394/LAN/Modem
INTB	LAN/Modem
INTC	VGA (Embedded in SIS650)
INTD	USB (Embedded in SIS961)

The table below summarizes the PCI bus master Allocation:

Arbiter	Signal	Agents (Master)	Function	Use
SIS 961	REQ00/GNT00	Realtek 8100BL	LAN Controller	
	REQ10/GNT10	OZ6912	Card Bus Controller	
	REQ20/GNT20	Agere 1648	MODEM Controller	
	REQ30/GNT30	Lucent FW 323	1394 controller	
	REQ40/GNT40	None	None	

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### 3.3.11 MBus Devices

The SMBus is a two-wire interface through which the system can communicate with power-related chips. The BIOS should initialize the SMBus devices during POST.

#### SIS961 SMBus Connection Devices

SMBus Device	Master/Slave	Address	BIOS Need to Initialization
SIS650 – Core Logic	Both Host and Slave	02h	Enable SMBus interface and SMBus interrupt
SO-DIMM	Slave	A0h	Not Need
ICS952001, ICS93722 CLK Generator	Slave	D2h	Program the desired clock frequency (Pin23 output 24MHz, Pin22 output 48MHz)

#### PMU08 SMBus Connection Devices

SMBus Device	Host/Slave	Address A7 ~ A1	BIOS Need to Initialization
PMU08	Master	10h	Enable PS01 decode interface
MAX1617 (Thermal sensor)	Slave	9Ch	Program the desired temperature range
Battery (1 <sup>st</sup> Battery)	Slave	A8h	No Need

### 3.3.12 Resource Allocation

This section summarizes the resource allocation of the notebook computer.

#### I/O Map

Hex Address	Device
000 – 01F	8237-1
020 – 021	8259-1
022	SIS 650 Control Register
02E – 02F	LPC-to-SIO interface
040 – 04D	8254
04E – 04F	LPC-to-SIO interface
060 – 064	Keyboard Controller
068 – 06C	PMU08
070 – 07F	RTC & NMI Mask
080 – 08F	DMA Page Registers
092	System Control Port
0A0 – 0A1	8259-2
Hex Address	Device

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0C0 – 0DF	8237-2
0F0 – 0FF	Math Coprocessor
170 – 177	Secondary IDE Controller
1F0 – 1F7	Primary IDE Controller
200 – 20F	Game Port
220 – 22F	Sound Blaster
279	PnP configuration – Address port
330 – 333	MIDI
370 – 371	Sound chip control port
378 – 37A	Parallel Port
388 – 38B	FM Synthesizer
398 – 399	Super I/O Chip
3B0 – 3DF	Video Controller
3E0 – 3E1	PCMCIA Controller
3E8 – 3EF	Fax/Modem
3F0 – 3F7	Floppy Disk Controller
3F8 – 3FF	Serial Port 1
530 – 537	Microsoft Sound System
778 – 77B	ECP port
A79	PnP configuration – Write data port
CF8 – CFC	PCI BUS configuration register

### I ISA DMA Map

DMA Channel	Device
DMA 0	Unused
DMA 1	ECP
DMA 2	Floppy Disk
DMA 3	Audio
DMA 4	[Cascade]
DMA 5	Unused
DMA 6	Unused
DMA 7	Unused

### I Memory Map

Address Range	Length	Description
00000 ~ 9FBFFh	640 KB	System Memory
9FC00 ~ 9FFFFh	128 KB	Video Memory
A0000 ~ BFFFFh	40 KB	Video ROM
C0000 ~ CFFFFh	72 KB	Unused
D0000 ~ DFFFFh	16 KB	DMI information

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E0000 ~ FFFFFh	128 KB	System ROM BIOS
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### IRQ Map

IRQ#	Description
IRQ 0	System Timer
IRQ 1	Keyboard
IRQ 2	[Cascade]
IRQ 3	PHS (Serial)
IRQ 4	Serial Port
IRQ 5	Audio/VGA/USB
IRQ 6	Floppy Disk Drive
IRQ 7	Parallel Port
IRQ 8	RTC Alarm
IRQ 9	Reserved for PCMCIA card
IRQ10	LAN / Modem or Combo, (Card Bus), IEEE 1394
IRQ11	ACPI
IRQ12	PS/2 Mouse
IRQ13	FPU (FERR)
IRQ14	Hard Disk Drive
IRQ15	CD-ROM or DVD-ROM

### 3.4 GPIO Pin Assignment

The GPI and GPO pins connected to system devices. The BIOS can get device's status and control the device via the GPI and GPO pins.

- SiS650 GPI pin assignment

GPIO Number	Signal Name	Default	I/O	Notes
GPIO0	LPC_PME0	1	I	0 : LPC_PME0 Event Enable 1 : normal operation
GPIO1	PMUFLASH0	1	O	0 : Flash PMU08 firmware 1 : normal operation
GPIO2	MB_ID0	1	I	0 : Mother Board ID0 Select 1 : normal operation
GPIO3	Q_SMI0	1	I	0 : External K/B SMI0 1 : normal operation
GPIO4	N.C.	--	--	--
GPIO5	GPRSFW_DET	1	I	0 : Updated GPRS F/W 1 : normal operation
GPIO6	N.C.	--	--	--
GPIO Number	Signal Name	Default	I/O	Notes

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GPIO7	EC_SCI0	1	I	0 : PMU SCI Detect 1 : PMU SCI Not Detect
GPIO8	PM_RI0	1	I	0 : wakeup event input enable 1 : wakeup event input disable
GPIO9	N.C.	--	--	--
GPIO10	MB_ID1	1	I	0 : Mother Board ID1 Select 1 : normal operation
GPIO11	PM_SLP_S10	1	O	0 : When system into S1 1 : normal operation
GPIO12	STPCPU0	1	O	0 : Stop CPU Clock 1 : normal operation
GPIO13	N.C.	--	--	--
GPIO14	SPDMUX0	1	O	SM BUS Select0
GPIO15	N.C.	--	--	--
GPIO16	N.C.	--	--	--
GPO17	N.C.	--	--	--
GPIO18	SPDMUX1	1	O	SM BUS Select1
GPIO19	ICH_SMBCLK	1	O	SM BUS Clock
GPIO20	ICH_SMBDATA	1	I/O	SM BUS Data

### 3.4.1 PMU08 GPIO Signal Description

PIN	Signal	I/O	Normal	Runtime / Wake event	Function
GPIOA0	LID#	I	LID Switch	Low = LCD Close.	Generate SMI/SCI
GPIOA1	N.C.	X			
GPIOA2	Mail LED#	O	Mail LED	Low = Mail Arrival	
GPIOA3	QGSMI#	I	M38869M8	Low = Keyboard SMI	
GPIOA4	PCMUTE#	O		Low = Mute PC speaker	Mute Speaker
GPIOA5	PSTMSK#	O		Low = PCI Reset Mask, Hi = PCI Reset Enable	Mask PCI power
GPIOA6	PCMRI#	I	OZ6912	Low = Ring Signal from PCMCIA	
GPIOA7	RI1#	I	Serial Port	Low = Ring Signal from Serial Port	
GPIOB0	N.C.	X			
GPIOB1	GPRS_SWE NA#	O		Low = GPRS Software Enable	
GPIOB2	N.C.	X			LED Select
GPIOB3	PDCOM#	O	MAX3243	Low = Power down RS232	Power down RS232
GPIOB4	N.C.	X			LAN Power On
PIN	Signal	I/O	Normal	Runtime / Wake event	Function
GPIOB5	N.C.	X			

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GPIOB6	PM_SLP_S1 #	I	SIS961	Low = POS, STR and STD suspend state	
GPIOB7	PM_RI#	O	SIS961	Low = Wake Up Event (SMI or SCI)	Generate SMI/SCI
GPIOC0	N.C.	X			
GPIOC1	N.C.	X			
GPIOC2	CHGLED	O	Charge LED	High = Turn ON Charge LED	Control charge LED
GPIOC3	N.C.	X			

I : INPUT O : OUTPUT L-Lever : Low Lever  
H-Lever : Hi Lever Function Pin Description :  
A : A-D Converter Input Pin

### 3.4.2 M38869 GPIO Signal Description

Address	Bit	r/w	Description	Remark
0060h	7:0	r	Read Data from Output Data Bus Buffer	
0060h	7:0	w	Write Data to into Input Data Bus Buffer	
0064h	7:0	r	Status	
0064h	7:0	w	Write Command into Input Data Bus Buffer	

Port Assign:

Port	Pin Name	In/Out	Description
PORT 0	P07 : P00	OUT	Key Scan Data Output
PORT 1	P17 : P10	OUT	Key Scan Data Output
PORT 3	P37 : P30	IN	Key Scan Data Input
PORT 2	P27	OUT	SCROLL Lock LED
	P26	OUT	NUM Lock LED
	P25	OUT	CAPS Lock LED
	P24	OUT	BLFN1
	P23	OUT	Wireless_RFON
	P22	OUT	NC
	P21	IN	PULL DOWN 1K ohm
	P20	OUT	NC
PORT 4	P46	OUT	NC
	P45	OUT	PULL UP 10Kohm
	P44	OUT	PULL UP 10Kohm
	P43	OUT	IRQ12
	P42	OUT	IRQ1
	P41	OUT	NC
	P40	OUT	KBCSMI0
Port	Pin Name	In/Out	Description
PORT 5	P57	OUT	NC



## Software Functional Overview

	P56	OUT	NC
	P55	IN	GPRS_PWRENA
	P54	IN	GPRS_VDDPD
	P50	OUT	ISA ADDRESS (SA2)
PORT 6	P61	IN	KBSEL2
	P60	IN	KBSEL1
	P62	IN	GPRS_ON/OFF
	P63	IN	LOGSEL
	P64	OUT	PASS0
	P65	IN	NC
	P66	OUT	BT_FETON1
	P67	OUT	BT_SENSE0
PORT 7	P70	I/O	PS2 DATA
	P73	I/O	PS2 CLOCK
	P72	I/O	EXTERNAL KB DATA
	P75	I/O	EXTERNAL KB CLOCK
	P74	I/O	EXTERNAL MOUSE CLOCK
	P71	I/O	EXTERNAL MOUSE DATA
	P76	I/O	SMDAT_KBC
	P77	I/O	SMCLK_KBC

**i** I : INPUT O : OUTPUT

# Software Functional Overview

## 3.5 Power Management

This section provides the Power Management software function of the notebook.

### 3.5.1 General Requirements

The BIOS meet the following general Power Management requirements:

- Compliant with ACPI 1.0B / ACPI 2.0 Specification
- Support for Suspend-to-RAM and Suspend-to-Disk mode
- Support for Resume on External Modem Ring while in S3 Mode
- Support for Resume on Internal Modem Ring while in S3 / S4 Mode
- Support for LAN Remote Power while in S3 / S4 Mode
- Power Management must not substantially affect or degrade system performance
- Power Management must be OS independent
- Support resume on Time/Date
- Support Wireless LAN wake up
- Support Internet / Mail button wake up

### 3.5.2 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
B+	Nil	IMM, (9V~12V)
+12V	PWRON	Inverter, AC97 codec, PCMCIA card
+3V	PWRON	VGA, Video RAM, PCMCIA, PCMCIA Slot 3V, DRAM, SIS 650 (DRAM I/F), MAX32443
+3VS	SUSB#	Firmware Hub, Audio, SIS 961 (ISA I/F Power), Clock Generator (IMI9827G SCLK), TAG RAM
+5V	PWRON	PCMCIA Slot 5V VCC, M38867
+5VS	SUSB#	Super I/O, HDD, CD-ROM, USB, LPT Port, Internal K/B, Glide Pad, External PS/2 Mouse, FDD, Audio AMP
+3V Always	Nil	uP (PMU08), SIS 961(RTC I/F), Internal modem ring

### 3.5.3 Power Management Mode

#### I Full On Mode

The system state where no devices are power managed and the system can respond to applications with maximum performance.

#### I Doze mode

The CPU clock is slow down and all other devices are full-on.

# Software Functional Overview

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## I Stand by mode

A suspend state where all motherboard components are still powered-on except for the system clock generator device. The PCI and CPU buses are driven to the inactive idle state. The system memory is powered and refreshed by the memory bridge, and the graphics frame buffer is powered and refreshed by the graphic chip. The system provides a 32Khz clock (SUSCLK) in this suspend mode to support refresh of these memory subsystems. Only an enabled “resume event” can bring the system out of the stand by state. The SIS 961 also provides a resume timer that allows the system to resume after a programmed time has elapsed.

## I Suspend to RAM mode (STR)

A suspend state where all motherboard components are powered-off. The CPU/L2 and PCI busses are powered off. All devices connected to the CPU/L2 and PCI busses must either be powered-off or isolate their bus interfaces. The system memory is powered and refreshed by the memory bridge, and the graphics frame buffer is powered and refreshed by the graphics chip. The system provides a 32 kHz clock (SUSCLK) in this suspend mode to support refresh of these memory subsystems. Only an enabled “resume event” can bring the platform out of the suspend to RAM (STR) state.

## I Suspend to Disk mode (STD)

A suspend state where the context of the entire system is saved to disk, all motherboard components are powered-off, and all clocks are stopped. Any enabled “resume event”, such as PowerBTN or RTC, can bring the platform out of the suspend to disk (STD) state.

## I Soft off mode (SOFF)

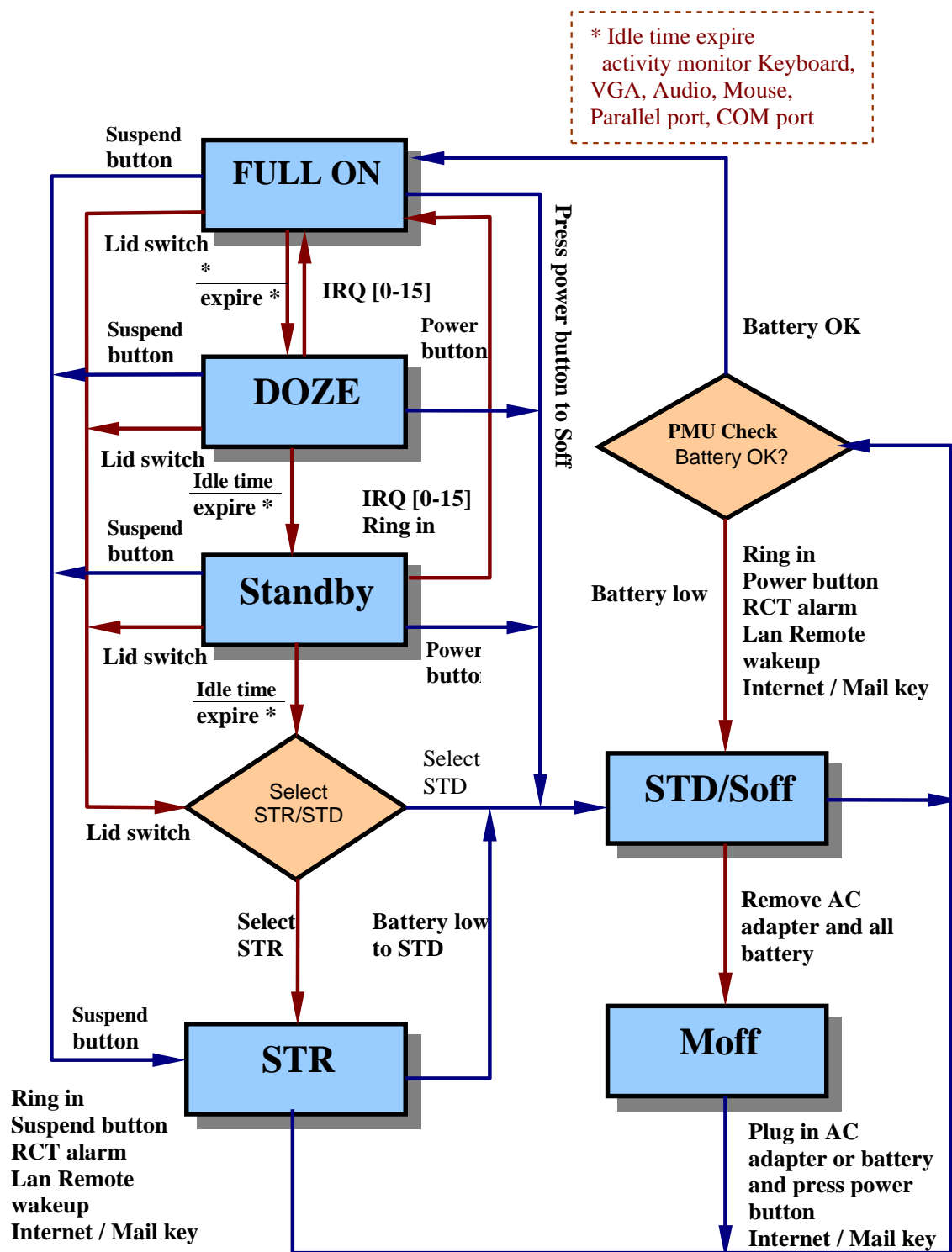
The This is the same as suspend to disk except the context of memory is not saved. The system will resume from Soft Off as if a hard reset had occurred.

## I Mechanical off mode

All power except the RTC has been removed from the system.

# Software Functional Overview

## 3.5.4 Power Management Mode Transition Flow



# Software Functional Overview

## 3.5.5 Power Management Mode Transition Event

The following table summarizes the entry events and wake-up events of each power

Power State	Entry Event	Wake up Event
Doze	Doze Time out	Predefined Mem/IO range access Ring Indicator Keystroke(Int., Ex. and USB keyboard) Mouse movement IRQ 1-15
Stand by	Stand by Time out	Predefined Mem/IO range access Battery Warning Battery Low Keystroke (Int., Ex. and USB keyboard ) Mouse movement
STR	Suspend Time out Lid close Power Button	Power Button Ring Indicator Schedule Alarm Battery Low Lid Open Internet / Mail key Mini-PCI Lan / Wireless Lan
STD	Suspend Time out Battery Low Power Button	Power Button Schedule Alarm Internet / Mail key Mini-PCI Lan / Wireless Lan
Soft Off	Power Button Execute Windows shutdown Command	Power Button Ring Indicator (By internal Modem only ) Schedule Alarm Internet / Mail key Mini-PCI Lan / Wireless Lan

## 3.5.6 Lid Switch

Display mode	Power State	Lid close		Lid open
		Backlight Off	STR	
LCD	Full on	Backlight Off	STR	Resume
	Stand by	Backlight Off	STR	Resume
	STR	No activity	No activity	Resume
CRT	Full on	No activity	No activity	No activity
	Stand by	No activity	No activity	No activity
	STR	No activity	No activity	Resume
Both	Full on	CRT	CRT	Both
	Stand by	CRT	CRT	Both
	STR	No activity	No activity	Resume

**i** If dual view enable lid close always suspend.

# Software Functional Overview

## 3.5.7 Power button and suspend button

Button	State					
	OFF	Full on	Doze	Stand by	STR	STD
Power	Power on	Power off	Power off	Full on	Full on	Full on
Suspend	Power on	STR/STD*	STR/STD	STR/STD	Full on	Full on

**i** As pressed Sleep button over 4~6 sec, the system will force to power off.

**i** \*The mode of STR/STD can be selected via CMOS setup.

## 3.5.8 Device Power management

### Power state of local devices table

PowerState Component	Doze	Stand By	STR	STD/Soff
CPU	Stop Grant	Stop Clock	Power Off	Power Off
SIS 650	ON	Stop Clock	Power Off (except Vcc)	Power Off
SIS 961	ON	ON	Power Off (except SUSVcc, RTCVcc )	Power Off (except SUSVcc, RTCVcc)
DRAM	ON	Self Refresh	Self Refresh	Power Off
L2 CACHE	ON	Power down	Power Off	Power Off
CDROM(DVD)	ON	Power down	Power Off	Power Off
HDD	ON	Power down	Power Off	Power Off
FDD	ON	Power down	Power Off	Power Off
KBC	ON	ON	Power ON	Power Off
PMU08	ON	ON	Suspend Mode	Suspend Mode
VGA/VRAM	ON	Power down	Power down	Power Off
Oz6912	ON	Power down	Power down	Power Off
Sound	ON	Power down	Power Off	Power Off
LCD Backlight	ON	Power down	Power Off	Power Off
Serial (UART1)	ON	Power down	Power down	Power Off
LAN	ON	Power down	Power down	Power Off
Modem	ON	Power down	Power down	Power down
Parallel	ON	Power down	Power Off	Power Off

# Software Functional Overview

## I Device PM control during Stand By mode

Device	Power Controlled by	Description
CPU	Hardware	Controlled by SUS_STAT1# pin
SIS 650/961	Hardware	Controlled by SUS_STAT1# pin
VGA Chip	Software	Controlled by BIOS call power down function
Super I/O Chip	Software	Controlled by BIOS send power down command
Keyboard Controller	Working	
FDD	Software	FDD support power down command
HDD	Software	HDD support power down command
CD-ROM	Software	CD-ROM support power down command
Audio Chip	Software	Controlled by Driver enter Dx State
Audio AMP	Software	Controlled by BIOS
Internal Modem	Software	Controlled by Driver enter Dx State
LAN	Software	Controlled by Driver enter Dx State
LCD Panel Backlight	Software	Controlled by BIOS set PMU08
Clock Synthesizer	Hardware	Controlled by CPUTSTP# and PCISTP# pin
PMU08	Working	
MAX3243	Software	Controlled by BIOS
L2 Cache	Software	Controlled by BIOS

## I Device PM control during STR mode

Device	Power Down Controlled by	Description
SIS 650 Core Logic	Hardware	Controlled by SIS 961, SUS_STAT1# pin
Super I/O	Hardware	Controlled by SUSB#
VGA Chip	Software	Controlled by System BIOS
HDD	Hardware	Controlled by SUSB#
CD-ROM	Hardware	Controlled by SUSB#
PCMCIA Controller	Hardware	Controlled by SUSB#
Internal Modem	Software	Controlled by Driver enter Dx State
LAN	Software	Controlled by Driver enter Dx State
FDD	Hardware	Controlled by SUSB#
Audio Chip	Software	Enter D3 Hot State
Audio AMP	Software	Controlled by BIOS set AC97 Codec
IR Module	Software	Controlled by BIOS set GPO[30]
LCD Panel	Hardware	Controlled by VGA Chip
Backlight	Software	Controlled by BIOS set PMU07
Clock Synthesizer	Hardware	Controlled by SUSB#
Keyboard Controller	Software	Controlled by BIOS send power down command
MAX3243	Software	Controlled by BIOS set GPO[13]
L2 Cache	Hardware	Controlled by SUSB# Pin
PMU08	Hardware	Controlled by SUSB# Pin

# Software Functional Overview

## I Device PM control during STD mode

Device	Power Down Controlled by	Description
SIS 650 Core Logic	Hardware	Power off
Super I/O	Hardware	Power off
VGA Chip	Hardware	Power off
HDD	Hardware	Power off
CD-ROM	Hardware	Power off
PCMCIA Controller	Hardware	Power off
Modem	Hardware	Support ring power
LAN	Hardware	Support Lan wakeup
FDD	Hardware	Power off
Audio Chip	Hardware	Power off
Audio AMP	Hardware	Power off
LCD Panel	Hardware	Power off
Backlight	Software	Controlled by BIOS set PMU07
Clock Synthesizer	Hardware	Power off
Keyboard Controller	Hardware	Power off
MAX3243	Hardware	Power off
L2 Cache	Hardware	Power off
PMU08	Hardware	Controlled by SUSC# Pin

## I The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
CPU Core	SUSB#	CPU's Core Part
CPU I/O	SUSB#	CPU's I/O Part, SRAM, SIS 650(CPU I/F), Clock Generator(CPU Clock)
+3V	PWRON	VGA, VideoRAM, PCMCIA, PCMCIA Slot 3V, DRAM, SIS 650(DRAM I/F), M3243
+3VS	SUSB#	FirmWare Hub, Audio, SIS 691(LPC I/F Power), Clock Generator (IMI9827G SCLK), TAG RAM
+5V	PWRON	PCMCIA Slot 5V VCC, M38867
+5VS	SUSB#	Super I/O, HDD, CD-ROM, USB, LPT Port, Internal K/B, Glide Pad, External P/S2 Mouse, IR, FDD, Audio AMP
+3V Always	Nil	PMU08 I/F, SIS 961(RTC I/F)



# Software Functional Overview

## 3.6 ACPI

This section provides the ACPI software function of the notebook.

### 3.6.1 General Requirements

The BIOS must meet the following general Power Management requirements:

- l Refers to the portion of the firmware that is compatible with the ACPI specifications.
- l Support for Suspend-to-RAM (S3 state) and Suspend-to-Disk mode (S4 state).
- l Support the Wake up event from External Modem Ring in S3 state. This controlled by a method \_PSW or Power Resource of \_PRW .
- l Support the Wake up event from LAN in S3~S5 state.
- l Support the Wake up event from Internal Modem in S3~S5 state.
- l Support the Wake up event from RTC Time/Date alarm in S3~S5 state.
- l Power Management must not substantially affect or degrade system performance.
- l Power Management must be OS independent.

### 3.6.2 System Power Plane

The system components are grouped as the following parties to let the system to control the On/Off of power under different power management modes.

The power plane is divided as following:

Power Group	Power Control Pin	Controlled Devices
B+	Nil	IMM, (9V~12V)
+12V	PWRON	Inverter, AC97 codec, PCMCIA card
+3V	PWRON	VGA, VideoRAM, PCMCIA, PCMCIA Slot 3V, DRAM, SIS 650(DRAM I/F), MAX32443
+3VS	SUSB#	FirmWare Hub, Audio, SIS 961(LPC I/F Power), Clock Generator (IMI9827G SCLK), TAG RAM
+5V	PWRON	PCMCIA Slot 5V VCC, M38867
+5VS	SUSB#	Super I/O, HDD, CD-ROM, USB, LPT Port, Internal K/B, Glide Pad, External PS/2 Mouse, FDD, Audio AMP
+3V Always	Nil	uP (PMU08),SIS 961 (RTC I/F), Internal modem ring

### 3.6.3 Global System State Definitions

Global system states (Gx states) apply to the entire system and are visible to the user. Global system states are defined by six principal criteria.

Following is a list of the system states:

#### l G0/S0 – Working

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed. The user will be able to select (through some user interface) various performance/power characteristics of the system to have the software optimize for performance or battery life. The system responds to external events in real time. It is not safe to disassemble the machine in this state.

# Software Functional Overview

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## I G1 - Sleeping

A computer state where the computer consumes a small amount of power, user mode threads are not being executed, and the system “appears” to be off (from an end user’s perspective, the display is off, etc). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state.

## I G2/S5 – Soft Off

A computer state where the computer consumes a minimal amount of power. No user mode or system mode code is running. This state requires a large latency in order to return to the Working state. The system’s context will not be preserved by the hardware. The system must be restarted to return to the Working state. It is not safe to disassemble the machine.

## I G3 – Mechanical Off

A computer state that is entered and left by a mechanical means. It is implied by the entry of this off state through a mechanical means that the no electrical current is running through the circuitry and it can be worked on without damaging the hardware or endangering the service personnel. The OS must be restarted to return to the Working state. No hardware context is retained. Except for the real time clock, power consumption is zero.

### 3.6.4 Sleeping State Definitions

Sleeping states (Sx states) are types of sleeping states within the global sleeping state, G1. The Sx states are briefly defined below. For a detailed definition of the system behavior within each Sx state and transition, refer to the ACPI specification.

#### I S1 Sleeping State

The S1 sleeping state is a low wake-up latency sleeping state. In this state, no system context is lost (CPU or chip set) and hardware maintains all system context.

#### I S2 Sleeping State

The S2 sleeping state is a low wake-up latency sleeping state. This state is similar to the S1 sleeping state except the CPU and system cache context is lost (the OS is responsible for maintaining the caches and CPU context). Control starts from the processor’s reset vector after the wake-up event.

#### I S3 Sleeping State (STR mode)

The S3 sleeping state is a low wake-up latency sleeping state where all system context is lost except system memory. CPU, cache, and chip set context are lost in this state. Hardware maintains memory context and restores some CPU and L2 configuration context. Control starts from the processor’s reset vector after the wake-up event.

#### I S4 Sleeping State (STD mode)

The S4 sleeping state is the lowest power, longest wake-up latency sleeping state supported by ACPI. In order to reduce power to a minimum, it is assumed that the hardware platform has powered off all devices. Platform context is saved in disk.

# Software Functional Overview

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## I S5 Soft Off State

The S5 state is similar to the S4 state except the OS does not save any context nor enable any devices to wake the system. The system is in the “SOFF” off state and requires a complete boot when awakened. Software uses a different state value to distinguish between the S5 state and the S4 state. This is to allow for initial boot operations within the BIOS to distinguish whether or not the boot is going to wake from a saved memory image.

### 3.6.5 Device Power State Definitions

#### Device # CPU K+

C0 Power State	-CPU executes instruction
C1 Power State	-CPU is in Auto Halt State
C2 Power State	-CPU is in Stop Clock mode
C3 Power State	-CPU is in Stop Clock mode

#### Device # HDD

D0 Power State	-HDD is accessing or idle
D1 Power State	-HDD is in standby mode -D1 is resumed by any access
D2 Power State	-HDD is in sleep mode -D2 is resumed by reset
D3 Power State	-Same with D2

#### Device # CD-ROM

D0 Power State	-CD-ROM is accessing or idle (motor on)
D1 Power State	-CD-ROM is in standby mode -D1 is resumed by any access
D2 Power State	-CD-ROM is in sleep mode -D2 is resumed by reset
D3 Power State	-Same with D2

#### Device # VGA

D0 Power State	-VGA is accessing or idle
D1 Power State	-VGA is in standby mode -D1 is resumed by any access
D2 Power State	-VGA is in suspend mode -D2 is resumed by access
D3 Power State	-Same with D2

#### Device # Modem

D0 Power State	-Modem is accessing or idle
D1 Power State	-Modem is in standby mode -D1 is resumed by any access
D2 Power State	-Same with D1
D3 Power State	-Same with D1

#### Device # PCMCIA

D0 Power State	-PCMCIA is accessing or idle
D1 Power State	-PCMCIA is in RUN# mode
D2 Power State	-PCMCIA is in suspend mode
D3 Power State	-Same with D2

## Software Functional Overview

Device # NIC

D0 Power State

-NIC is accessing or idle

D1 Power State

-Snooze is in CLKRUN is asserted

D2 Power State

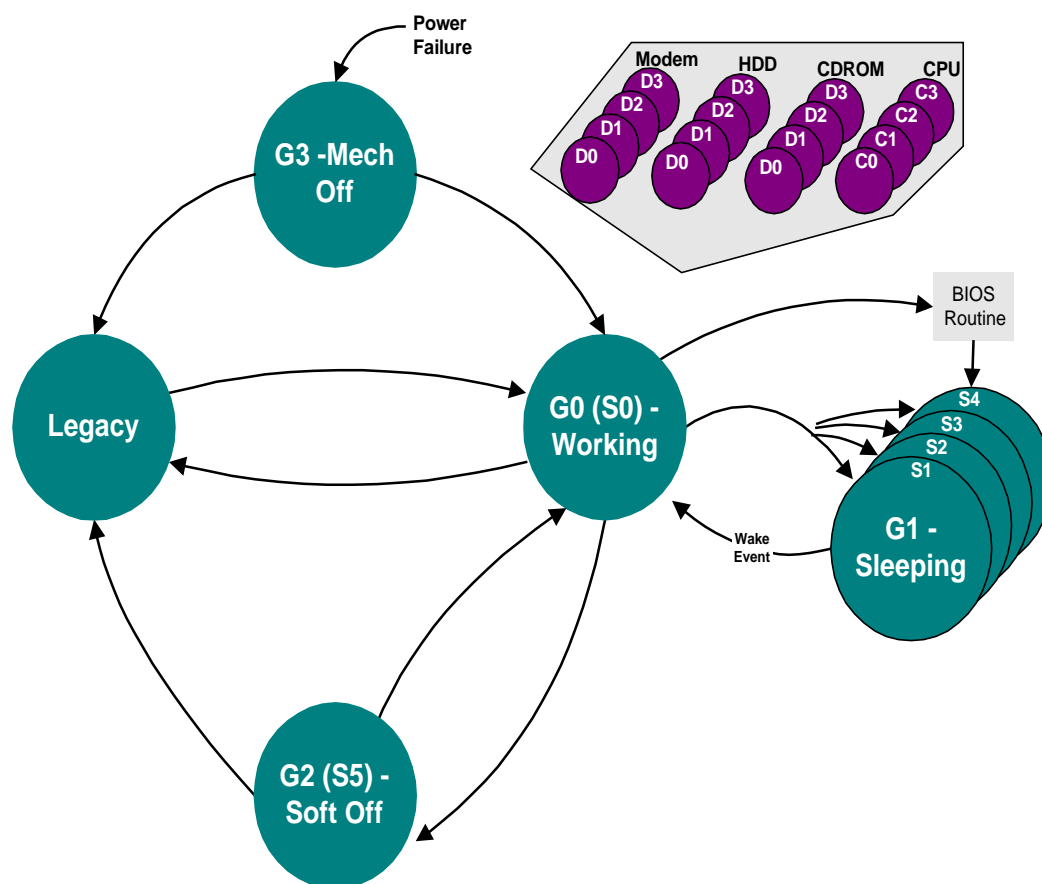
-Sleep mode, PCI chip in suspend mode

D3 Power State

-Power down mode, both PCI and phyter in sleep mode.

### 3.6.6 Power Management Transition Flow Chart

From a user-visible level, the system can be thought of as being one of the states in the following diagram:



## Software Functional Overview

### 3.6.7 Power States transition event

The following table summarizes the entry events and wake-up events of each power:

Power State	Entry Event	Wake up Event
S1	OSPM* control	Predefined Mem/IO range access Ring Indicator Keystroke IRQ1-15 SMI# / ACPI SCI# / USB
S2	OSPM control	Predefined Mem/IO range access Battery Warning / Battery Low Ring Indicator Keystroke (Int., Ex. And USB keyboard ) Mouse movement Schedule Alarm SMI# / ACPI SCI# / USB
S3	OSPM control, Sleep Button, Lid Close	Power button Ring Indicator Schedule Alarm Lid Open PME# Battery Low Lan Remote power on Internet / Mail key
S4	OSPM control, Sleep Button	Power Button Ring Indicator Schedule Alarm Lan Remote Power on PME# Internet / Mail key
S5	OSPM control	Power Button Internet / Mail Key

**i** [OSPM: OS-directed Power Management](#)

### 3.6.8 Lid Switch

The function of Lid Switch depends on the ACPI aware OS.

Display mode	Power States	Lid Close	Lid Open
LCD	G0	S3	G0
	S1~S2	S3	Go
	S3~S5	No active	No active
CRT	G0	No active	No active
	S1~S2	No active	No active
	S3~S5	No active	No active
SIMUL	G0	CRT	No active
	S1~S2	CRT	No active
	S3~S5	No active	No active

**i** [If dual view enable lid close always suspend.](#)

## Software Functional Overview

### 3.6.9 Power Button and Internet / Mail Button

The function of Power/Sleep Button is depends on the ACPI aware OS.

Button	State					
	G0	S1	S2	S3	S4	S5
Power	Power off	Power off	Power off	No active	No active	G0
Internet / Mail Key	No active	G0	G0	G0	G0	Go

**i** \*Press power and suspend button reset PIC

### 3.6.10 Device Power Control Methodology

This section illustrates the power control status of each key device/component of the system under each power management mode.

#### I Power state of local devices table

PowerState Component	S1	S2	S3	S4/S5
CPU	Stop Grant	Stop Clock	Power Off	Power Off
SIS 650	ON	Stop Clock	Power Off (except Vcc)	Power Off
SIS 961	ON	ON	Power Off (except SUSVcc, RTCVcc )	Power Off (except SUSVcc, RTCVcc)
DRAM	ON	Self Refresh	Self Refresh	Power Off
L2 CACHE	ON	Power down	Power Off	Power Off
CDROM(DVD)	ON	Power down	Power Off	Power Off
HDD	ON	Power down	Power Off	Power Off
FDD	ON	Power down	Power Off	Power Off
KBC	ON	ON	Power down	Power Off
PMU08	ON	ON	Power ON	Power down
VGA/VRAM	ON	Power down	Power down	Power Off
Oz6912 (PCMCIA)	ON	Power down	Power down	Power Off
Sound	ON	Power down	Power Off	Power Off
LCD Backlight	ON	Power Off	Power Off	Power Off
Serial (UART1)	ON	Power down	Power down	Power Off
LAN	ON	Power down	Power down	Power Off
Modem	ON	Power down	Power down	Power down
Parallel	ON	Power down	Power Off	Power Off

# Software Functional Overview

## I Device PM control during Stand By mode

Device	Power Controlled by	Description
CPU	Hardware	Controlled by SUS_STAT1# pin
SIS 650/961	Hardware	Controlled by SUS_STAT1# pin
VGA Chip	Software	Controlled by BIOS call power down function
PCMCIA Controller	Software	Controlled by Driver enter Dx State
Super I/O Chip	Software	Controlled by BIOS send power down command
Keyboard Controller	Working	
FDD	Software	FDD support power down command
HDD	Software	HDD support power down command
CD-ROM	Software	CD-ROM support power down command
Audio Chip	Software	Controlled by Driver enter Dx State
Audio AMP	Hardware	Controlled by BIOS set AC97 Codec
Internal Modem	Software	Controlled by Driver enter Dx State
LAN	Software	Controlled by Driver enter Dx State
LCD Panel Backlight	Software	Controlled by BIOS set PMU07
Clock Synthesizer	Hardware	Controlled by CPUTP# and PCISTP# pin
PMU08	Working	
MAX3243	Software	Controlled by BIOS ASL code
L2 Cache	Hardware	Controlled by BIOS

## I Device PM control during STR mode

Device	Power Down Controlled by	Description
SIS 650Core Logic	Hardware	Controlled by SIS 961, SUS_STAT1# pin
Super I/O	Hardware	Controlled by SUSB#
VGA Chip	Software	Controlled by VGA Driver enter D3 Hot
HDD	Hardware	Controlled by SUSB#
CD-ROM	Hardware	Controlled by SUSB#
PCMCIA Controller	Hardware	Controlled by SUSB#
LAN	Software	Controlled by Driver enter D3 Hot Sate
FDD	Hardware	Controlled by SUSB#
Audio Chip	Software	Enter D3 Hot State
Audio AMP	Hardware	Controlled by BIOS set AC97 Codec
LCD Panel	Hardware	Controlled by VGA Chip
Backlight	Software	Controlled by BIOS set PMU08
Clock Synthesizer	Hardware	Controlled by SUSB#
Keyboard Controller	Software	Controlled by BIOS send power down command
MAX3243	Hardware	Controlled by BIOS ASL code
L2 Cache	Hardware	Controlled by SUSB# Pin
PMJU08	Software	Controlled by SUSB# Pin

# Software Functional Overview

## I Device PM control during STD mode

Device	Power Down Controlled by	Description
SIS 650 Core Logic	Hardware	Power off
Super I/O	Hardware	Power off
VGA Chip	Hardware	Power off
HDD	Hardware	Power off
CD-ROM	Hardware	Power off
PCMCIA Controller	Hardware	Power off
LAN	Hardware	Power off
FDD	Hardware	Power off
Audio Chip	Hardware	Power off
Audio AMP	Hardware	Power off
LCD Panel	Hardware	Power off
Backlight	Software	Controlled by BIOS set PMU08
Clock Synthesizer	Hardware	Power off
Keyboard Controller	Hardware	Power off
MAX3243(RS232 transceiver )	Hardware	Power off
L2 Cache	Hardware	Power off
PMU08	Software	Controlled by SUSC#

## I The power plane is divided as following:

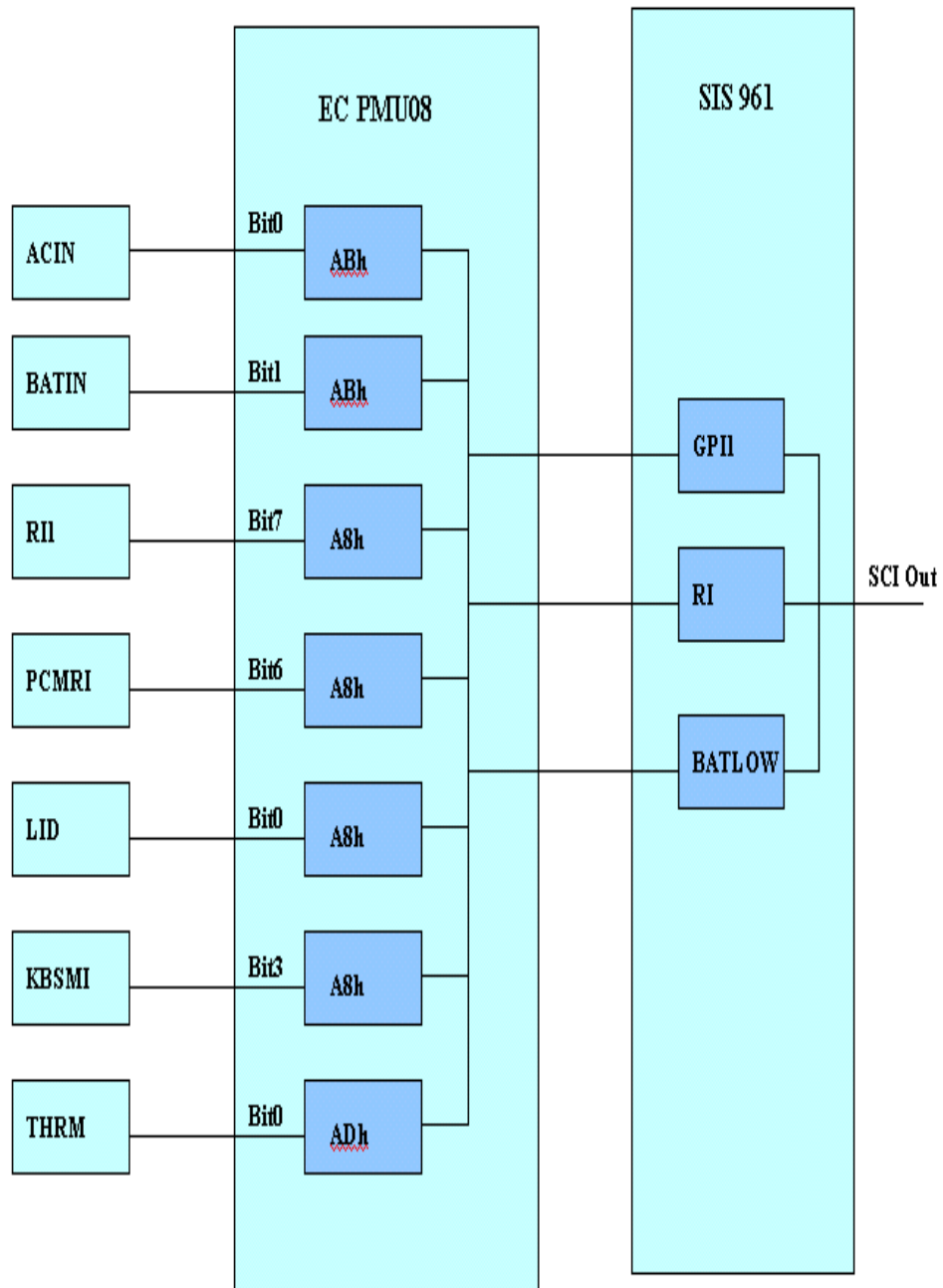
Power Group	Power Control Pin	Controlled Devices
CPU Core	SUSB#	CPU's Core Part
CPU I/O	SUSB#	CPU's I/O Part, SRAM, SIS 650(CPU I/F), Clock Generator(CPU Clock)
+3V	PWRON	VGA, VideoRAM, PCMCIA, PCMCIA Slot 3V, DRAM, SIS 650(DRAM I/F), MAX32443
+3VS	SUSB#	Flash ROM, Audio, SIS 961(LPC I/F Power), Clock Generator (IMI9827G SCLK), TAG RAM
+5V	PWRON	PCMCIA Slot 5V VCC, M38867
+5VS	SUSB#	Super I/O, HDD, CD-ROM, USB, LPT Port, Internal K/B, Glide Pad, External P/S2 Mouse, IR, FDD, Audio AMP
+3V Always	Nil	uP (PMU08), SIS 961(RTC I/F)



## Software Functional Overview

### 3.6.11 Expanding Event Through the Embedded Controller

The following figure shows the relationships between the devices that are wired to the embedded controller, the embedded controller queries, and ACPI general



# Software Functional Overview

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## I SCI Source and Query Event from M38867

PMU08	Input Event	GPE Event	Handler
ADPIN#	AC Plug In/Out	GPI1	AML Handler
BAT0#	Battery Plug In/Out	GPI1	AML Handler
GPIOA0	LID Event	RI	AML Handler
GPIOA3	Keyboard SMI	RI	AML Handler
GPIOA6	PCMCIA Ring In	RI	AML Handler
GPIOA7	COM Port Ring In	RI	AML Handler
THRM	Thermal Event	GPI1	AML Handler

The system will issue a beep to inform user while the following SCI alerted:

- § AC (AC status change) update battery information.
- § BAT ( Battery status change) update battery information.
- § Lid (Lid close/open event) update Lid position status.
- § RI10 COM Port Ring Event
- § PCMRI10 PCMCIA Ring Event
- § THRM0 (Thermal event) update thermal level information

## I Control Method Battery Subsystem

EC should support all the battery information to ACPI-OS

- Designed Battery capacity
- Designed Voltage
- Designed Low battery capacity
- Designed Low – Low battery capacity
- Latest Full charged capacity
- Present Remaining capacity
- Present drain rate
- Present voltage
- Present Battery Status

ACPI BIOS should support an independent device object in the name space, and implement the following methods.

# Software Functional Overview

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## I Battery Control Methods

Object	Description
_BIF	Return static information about a battery (i.e., model number, serial number, design voltage, etc.)
_BST	Returns the current battery status (i.e., dynamic information about the battery such as whether the battery is currently charging, an estimate of the remaining battery capacity, etc.).
_BTP	Sets the Battery Trip point, which generates an SCI when the battery(s) capacity reaches the specified point
_PCL	List of pointers to the device objects representing devices powered by the battery.
_STA	Returns general status of the battery (for a description of the _STA control method.

### 3.6.12 Thermal Control

ACPI allows OS to be proactive in its system cooling policies. With OS in control of the operating environment, cooling decisions can be made based on application load on the CPU and the thermal heuristics of the system. Graceful shutdown of OS at critical heat levels becomes possible as well. The following sections describe the thermal objects available to OS to control platform temperature. ACPI expects all temperatures to be given in tenths of Kelvin.

The ACPI thermal design is based around regions called *thermal zones*. Generally, the entire PC is one large thermal zone, but an OEM can partition the system into several thermal zones if necessary.

## I Active, Passive, and Critical Policies

There are three primary cooling policies that the OS uses to control the thermal state of the hardware. The policies are *Active*, *Passive* and *Critical*:

- **Passive cooling:** The OS reduces the power consumption of the system to reduce the thermal output of the machine by slowing the processor clock. The \_PSV control method is used to declare the temperature to start passive cooling.
- **Active cooling:** The OS takes a direct action such as turning on a fan. The \_ACx control methods declare the temperatures to start different active cooling levels.
- **Critical trip point:** This is the threshold temperature at which the OS performs an orderly, but critical, shut down of the system. The \_CRT object declares the critical temperature at which the OS must perform a critical shutdown.

When a thermal zone appears, the OS runs control methods to retrieve the three temperature points at which it executes the cooling policy. When the OS receives a thermal SCI it will run the \_TMP control method, which returns the current temperature of the thermal zone. The OS checks the current temperature against the thermal event temperatures. If \_TMP is greater than or equal to \_ACx then the OS will turn on the associated active cooling device(s). If \_TMP is greater than or equal to \_PSV then the OS will perform CPU throttling. Finally if \_TMP is greater than or equal to \_CRT then the OS will shutdown the system.

# Software Functional Overview

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An optimally designed system that uses several SCI events can notify the OS of thermal increase or decrease by raising an interrupt every several degrees. This enables the OS to anticipate `_ACx`, `PSV`, or `_CRT` events and incorporate heuristics to better manage the systems temperature. The operating system can request that the hardware change the priority of active cooling vs passive cooling.

## I Dynamically Changing Cooling Temperatures

An OEM can reset `_ACx` and `_PSV` and notify the OS to reevaluate the control methods to retrieve the new temperature settings. The following three causes are the primary uses for this thermal notification:

- When a user changes from one cooling mode to the other.
- When a swappable bay device is inserted or removed. A swappable bay is a slot that can accommodate several different devices that have identical form factors, such as a CD-ROM drive, disk drive, and so on. Many mobile PCs have this concept already in place.
- When the temperature reaches an `_ACx` or the `_PSV` policy settings

In each situation, the OEM-provided AML code must execute a **Notify** (`thermal_zone`, 0x80) statement to request the OS to re-evaluate each policy temperature by running the `_PSV` and `_ACx` control methods.

### n Resetting Cooling Temperatures from the User Interface

When the user employs the UI to change from one cooling mode to the other, the following occurs:

1. The OS notifies the hardware of the new cooling mode by running the Set Cooling Policy (`_SCP`) control method.
2. When the hardware receives the notification, it can set a new temperature for both cooling policies and notify the OS that the thermal zone policy temperatures have changed.
3. The OS re-evaluates `_PSV` and `_ACx`.

### n Resetting Cooling Temperatures to Adjust to Bay Device Insertion or Removal

The hardware can adjust the thermal zone temperature to accommodate the maximum operating temperature of a bay device as necessary. For example,

1. Hardware detects that a device was inserted into or removed from the bay and resets the `_PSV` and/or `_ACx` and then notifies the OS of the thermal and device insertion events.
2. The OS reenumerates the devices and reevaluates `_PSV` and `_ACx`.

### n Resetting Cooling Temperatures to Implement Hysteresis

An OEM can build hysteresis into platform thermal design by dynamically resetting cooling temperatures. For example,

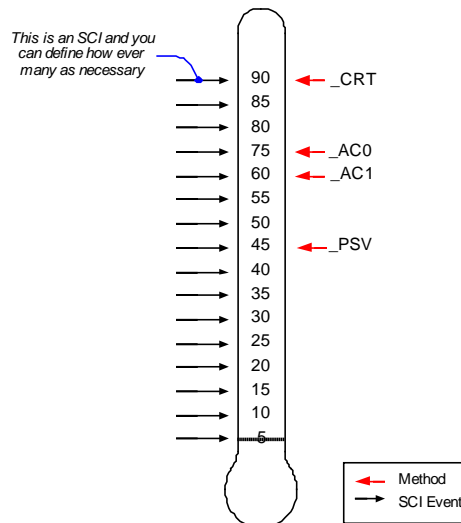
# Software Functional Overview

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1. When the heat increases to the temperature designated by `_ACx`, the OS will turn on the associated active cooling device and the hardware will reset the `ACx` value to a lower temperature.
2. The hardware will then run the `Notify` command and the OS will reevaluate the new temperatures. Because of the lower `_ACx` value now, the fan will be turned off at a lower temperature than when turned on.
3. When the temperature hits the lower `_ACx` value, the OS will turn off the fan and reevaluate the control methods when notified.

## 3.6.13 Hardware Thermal Events

An ACPI-compatible OS expects the hardware to generate a thermal event notification through the use of the SCI. When the OS receives the SCI event, it will run the `_TMP` control method to evaluate the current temperature. Then the OS will compare the value to the cooling policy temperatures. If the temperature has crossed over one of the three policy thresholds, then the OS will actively or passively cool (or stop cooling) the system, or shutdown the system entirely.



Both the number of SCI events to be implemented and the granularity of the temperature separation between each SCI event is OEM-specific. However, it is important to note that since the OS can use heuristic knowledge to help cool the system, the more events the OS receives the better understanding it will have of the system thermal characteristic.

## 3.6.14 Active Cooling Strength

The Active cooling methods (`_ACx`) in conjunction with active cooling lists (`_ALx`), allows an OEM to use a device that offers varying degrees of cooling capability or multiple cooling devices. The `_ACx` method designates the temperature at which the Active cooling is enabled or disabled (depending upon the direction in which the temperature is changing). The `_ALx` method evaluates to a list of devices that actively cool the zone. For example:

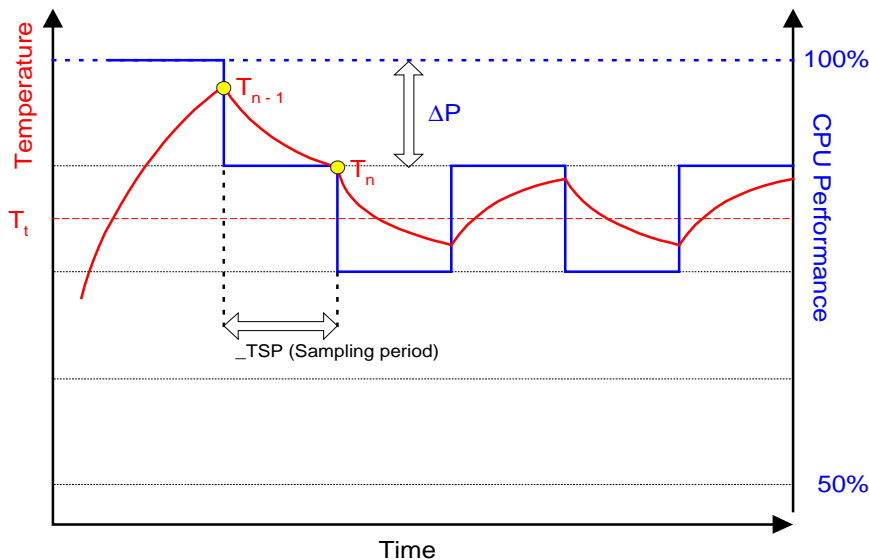
- If a standard single-speed fan is the Active cooling device, then the policy is represented by the temperature to which `_AC0` evaluates, and the fan is listed in `_AL0`.

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- If the zone uses two independently-controlled single-speed fans to regulate the temperature, then \_AC0 will evaluate to the maximum cooling temperature using two fans, and \_AC1 will evaluate to the standard cooling temperature using one fan.
- If a zone has a single fan with a low speed and a high speed, the \_AC0 will evaluate to the temperature associated with running the fan at high-speed, and \_AC1 will evaluate to the temperature associated with running the fan at low speed. \_AL0 and \_AL1 will both point to different device objects associated with the same physical fan, but control the fan at different speeds.

### 3.6.15 Passive Cooling Equation

Unlike the case for \_ACx, during passive cooling the OS takes the initiative to actively monitor the temperature in order to cool the platform. On an ACPI-compatible platform that properly implements CPU throttling, the temperature transitions will be similar to the following figure.



For the OS to assess the optimum CPU performance change required to bring the temperature down, the following equation must be incorporated into the OS.

$$\Delta P [\%] = \_TC1 * (T_n - T_{n-1}) + \_TC2 * (T_n - T_t)$$

where

$T_n$  = current temperature

$T_t$  = target temperature (\_PSV)

The two coefficients \_TC1 and \_TC2 and the sampling period \_TSP are hardware-dependent constants the OEM must supply to the OS (for more information, see section 12.3). The object \_TSP contains a time interval that the OS uses to poll the hardware to sample the temperature. Whenever \_TSP time has elapsed, the OS will run \_TMP to sample the current temperature (shown as  $T_n$  in the above equation). Then the OS will use the sampled temperature and \_PSV (which is the target temperature  $T_t$ ) to evaluate the equation for  $\Delta P$ . The granularity of  $\Delta P$  is determined by the CPU duty width of the system. A detailed explanation of this thermal feedback equation is beyond the scope of this specification.

# Software Functional Overview

## 3.6.16 Critical Shutdown

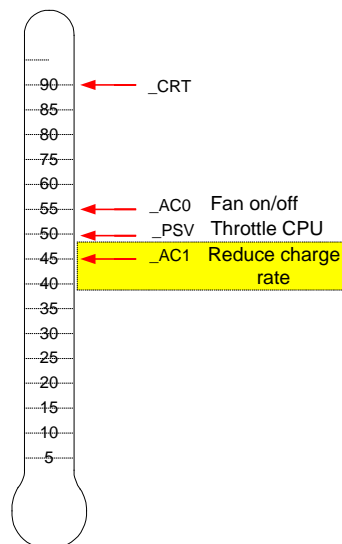
When the heat reaches the temperature indicated by `_CRT`, the OS must immediately shutdown the system. The system must disable the power either after the temperature reaches some hardware-determined level above `_CRT` or after a predetermined time has passed. Before disabling power, platform designers should incorporate some time that allows the OS to run its critical shutdown operation. There is no requirement for a minimum shutdown operation window that commences immediately after the temperature reaches `_CRT`. This is because

- Heat might rise rapidly in some systems and slower on others, depending on casing design and environmental factors.
- Shutdown can take several minutes on a server and only a few short seconds on a hand-held device.

Because of this indistinct discrepancy and the fact that a critical heat situation is a remarkably rare occurrence, ACPI does not specify a target window for a safe shutdown. It is entirely up to the OEM to build in a safe buffer that it sees fit for the target platform.

## 3.6.17 Other Implementation of Thermal Controllable Devices

The ACPI thermal event model is flexible enough to accommodate control of almost any system device capable of controlling heat. For example, if a mobile PC requires the battery charger to reduce the charging rate in order to reduce heat it can be seamlessly implemented as an ACPI cooling device. Associating the charger as an active cooling device and reporting to the OS target temperatures that will enable or disable the power resource to the device do this. Figure as following illustrates the implementation. Because the example does not create noise, this will be an implementation of *silence* mode.



# Software Functional Overview

## 3.6.18 Thermal Control Methods

Control methods and objects related to thermal management are listed in the table below.

Object	Description
_ACx	Returns Active trip point in tenths Kelvin
_ALx	List of pointers to active cooling device objects
_CRT	Returns critical trip point in tenths Kelvin
_PSL	List of pointers to passive cooling device objects
_PSV	Returns Passive trip point in tenths Kelvin
_SCP	Sets user cooling policy (Active or Passive)
_TC1	Thermal constant for Passive cooling
_TC2	Thermal constant for Passive cooling
_TMP	Returns current temperature in tenths Kelvin
_TSP	Thermal sampling period for Passive cooling in tenths of seconds

### I \_ACx

This control method returns the temperature at which the OS must start or stop Active cooling, where  $x$  is a value between 0 and 9 that designates multiple active cooling levels of the thermal zone. If the Active cooling device has one cooling level (that is,  $n=1$ ) then that cooling level is named \_AC0. If the cooling device has two levels of capability, such as a high fan speed and a low fan speed, then they are named \_AC0 and \_AC1 respectively. The smaller the value of  $x$ , the greater the cooling strength \_AC $x$  represents. In the above example, \_AC0 represents the greater level of cooling (the faster fan speed) and \_AC1 represents the lesser level of cooling (the slower fan speed). For every AC $x$  method, there must be a matching AL $x$  method.

Arguments: None.

Result Code: Temperature in tenths Kelvin

The result code is an integer value that describes up to 0.1 precisions in Kelvin. For example, 300.0K are represented by the integer 3000.

### I \_ALx

This object evaluates to a list of Active cooling devices to be turned on when the associated \_AC $x$  trip point is exceeded. For example, these devices could be fans.

### I \_CRT

This control method returns the critical temperature at which the OS must shutdown the system.

Arguments: None.

Result Code: Temperature in tenths Kelvin

The result is an integer value that describes up to 0.1 precisions in Kelvin. For example,



# Software Functional Overview

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300.0K are represented by the integer 3000.

## I    \_PSL

This object evaluates to a list of processor objects to be used for Passive cooling.

## I    \_PSV

This control method returns the temperature at which the OS must activate CPU throttling.

Arguments: None.

Result Code: Temperature in tenths Kelvin.

The result code is an integer value that describes up to 0.1 precision in Kelvin. For example, 300.0 Kelvin is represented by 3000.

## I    \_SCP

This control method notifies the hardware of the current user cooling mode setting. The hardware can use this as a trigger to reassign \_ACx and \_PSV temperatures. The operating system will automatically evaluate \_ACx and \_PSV objects after executing \_SCP.

Arguments: 0 - Active; 1 - Passive

Result Code: None.

## I    \_TC1

This is a thermal object that evaluates to the constant \_TC1 for use in the Passive cooling formula:

$$\Delta\text{Performance} [\%] = \_TC2 * (T_n - T_{n-1}) + \_TC1 * (T_n - T_t)$$

## I    \_TC2

This is a thermal object that evaluates to the constant \_TC2 for use in the Passive cooling formula:

$$\Delta\text{Performance} [\%] = \_TC2 * (T_n - T_{n-1}) + \_TC1 * (T_n - T_t)$$

## I    \_TMP

This control method returns the thermal zone      current operating temperature in Kelvin.

Argument: None.

Result Code: Temperature in tenths Kelvin.

The result is an integer value that describes up to 0.1 precision in Kelvin. For example, 300.0K is represented by the integer 3000.

## I    \_TSP

This is an object that evaluates to a thermal sampling period used by the OS to implement the Passive cooling equation. This value, along with \_TC1 and \_TC2, will enable the OS to provide the proper hysteresis required by the system to accomplish an effective passive cooling policy. The granularity of the sampling period is 0.1second. For example, if the sampling period is 30.0 seconds, then \_TSP needs to report 300; if the sampling period is 0.5 seconds, then it will report 5. The OS can normalize the sampling over a longer period if necessary.

# Software Functional Overview

## 3.6.19 AC Adapters and Power Source Objects

The Power Source objects describe the power source used to run the system.

Object	Description
_PSR	Returns present power source device
_PCL	List of pointers to powered devices.

### I \_PSR

Returns the current power source devices. Used for the AC adapter and is located under the AC adapter object in name space. Used to determine if system is running off the AC adapter.

Arguments: None

**Results code:** 0x00000000 = Off-line; 0x00000001 = On-line

### I \_PCL

This object evaluates to a list of pointers, each pointing to a device or a bus powered by the power source device. Pointing a bus means that all devices under the bus is powered by it power source device.

## 3.7 Battery Management

This notebook supports only Li-Ion Battery Pack. There is only one battery pack activating at one time. The special designed Bridge Battery module can backup the system under Suspend To RAM mode for a short period of time.

### 3.7.1 Battery Sub-system

The charger will stop charge the battery when the following condition is detected.

- The temperature of the system is too high
- Battery reading methodology is through PMU08 SMBus
- Battery Life is around 2.5 to 3 Hours.(T.B.D)

**i** Note that the battery life depends on different configuration running. (e.g. the battery life is shorter with CDROM running, the battery life is longer with document keyin only; battery life is short while PMU disabled, battery life is longer while PMU enabled.)

### 3.7.2 Battery Low Warning

When the battery capacity remains 8%, the PMU08 will generate a battery warning SMI. The system will do the following action.

- The Power LED Indicator will continually blinking with 1 Hz.
- The system issues a warning beep (3 beeps at once)

### 3.7.3 Battery Low

When the battery capacity remains 3%, the system will generate a battery low SMI. The system will do the following action.

# Software Functional Overview

- The system will enter Suspend To Disk mode even the power management is disabled. The function of power-on or Resume will be inhibited until the battery low condition is removed.

## 3.7.4 AC Adapter

When plug in the AC adapter, the system will do the following action:

- The charger will charge the battery if it is possible.
- The Battery Charging Indicator will turn on if the battery is in changing mode.
- The power management function will be disabled, if the Setup item of “Power Management Mode” is set to “Battery Only”

## 3.8 PMU08

The embedded controller PMU08 acts as a supplement for power management control. It supports a lot of functions via SMBus interface.

### 3.8.1 The System EC RAM With PMU08

Embedded Controller Command Set

The EC I/F command set allows the OS to communicate with the PMU08.

For detail information refer to ACPI 1.0B specification.

EC I/F Command	Command Byte Encoding	Byte	Register	R / W	Description	Interrupt
Read Embedded Controller (RD_EC)	0x80	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
		#2	EC_DA TA	W	Address byte to read	No Interrupt
		#3	EC_DA TA	R	Read data to host	Interrupt on OBF=1
Write Embedded Controller (WR_EC)	0x81	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
		#2	EC_DA TA	W	Address byte to write	Interrupt on IBF=0
		#3	EC_DA TA	W	Data to write	Interrupt on IBF=0
Burst Enable Embedded Controller (BE_EC)	0x82	#1	EC_SC	W	Command byte Header	No Interrupt
		#2	EC_DA TA	R	Burst acknowledge byte	Interrupt on OBF=1
Burst Disable Embedded Controller (BD_EC)	0x83	#1	EC_SC	W	Command byte Header	Interrupt on IBF=0
Query Embedded	0x84	#1	EC_SC	W	Command byte Header	No Interrupt

## Software Functional Overview

Controller (QR_EC)		#2	EC_DA TA	R	Query value to host	Interrupt on OBF=1
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### 3.8.2 PMU08 EC RAM List

The micro controller PMU08 acts as a supplement for power management control. It supports the following functions via SMBus Command ( **0x80** , **0xC0** )

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
1 <sup>st</sup> Battery [ _BIF ]	00h *3	Power unit	R(/W)	DATA[15:0] *1								-	0xffff	0x0000: mWh [Fixed value] 0xffff: Unknown
	02h *3	Design capacity	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	04h *3	Last Full Charge Capacity	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	06h *3	Battery Technology	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 : Primary 0x0001: Secondary [Fixed value] 0xffff: Unknown.
	08h *3	Design Voltage	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mV) 0xffff: Unknown
	0Ah *3	Design capacity of Warning	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	0Ch *3	Design capacity of Low	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	0Eh *3	Battery capacity Granularity 1	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	10h *3	Battery capacity Granularity 2	R(/W)	DATA[15:0] *1								-	0xffff	0x0000-0xffff(mWh) 0xffff: Unknown
	12h *3	Model number	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]
	14h *3	Serial Number	R(/W)	DATA[15:0] *1								-	0xffff	0x0000 [Not support]
	16h *3	Battery type	R(/W)	DATA[15:8] *1 All bits are 0				CELL_TY P E [7:0]				-	0xffff	CELL_ TYPE [3:0] This code depends on battery data format. In the future, this code may be added. 0x00: NiMH 0x01: Li-ion 0x10: Non-rechargeable battery (Reserved)
	18h *3	OEM Information	R(/W)	DATA [15:8] *1 All bits are 0				Vender[7:0]				-	0xffff	Vender [7:0] This code depends on battery data format. And the following name should be described in the ASL with the same character code. In the future, these codes will be added. 0: "MoliEnergy" 1: "Panasonic" 2: (SANYO does not agree the vender name display) 3: "TBCL" (Toshiba) 4: "Sony"

\*1: The register type is word.

\*3: This register is not cleared if the system is in S4-S5 state.

R(/W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
1 <sup>st</sup> Battery [ _BST ]	1Ah *3	Battery State	R/(W)	DATA[15:3] *1 All bits are 0					C R I T	C H G	D C H G	-	-	DCHG=1: The battery is discharged CHG =1 : The battery is charged CRIT =1 : The battery is critical (Empty)
	1Ch *3	Battery Present rate	R/(W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mW) 0xffff: Unknown
	1Eh *3	Battery Remaining Capacity	R/(W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mWh) 0xffff: Unknown
	20h *3	Battery present Voltage	R/(W)	DATA[15:0] *1								-	0xffff	0x0000-0xfffe(mV) 0xffff: Unknown
1 <sup>st</sup> Battery [ _BTP ]	22h	Battery Trip Point	R/W	DATA[15:0] *1								-	0x0000	0x0000 :Clear the trip point 0x0001-0xffff(mWh)
2 <sup>nd</sup> Battery [ _BIF ]	24h to 3Ch *3	*2	*2	*2								*2	*2	*2
2 <sup>nd</sup> Battery [ _BST ]	3Eh to 44h *3	*2	*2	*2								*2	*2	*2
2 <sup>nd</sup> Battery [ _BTP ]	46h	*2	*2	*2								*2	*2	*2
-	48h	Battery data Size	R/(W)	DATA[7:0]								-	-	0x01 : DATA size is 3byte.(PMU06A) 0x00 :DATA size is 2 byte. (PMU06) *8
1 <sup>st</sup> Battery [ _BIF ]	49h	Design capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 02/03h. *7 *8
	4Ah	Last Full Charge Capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 04/05h. *7 *8
1 <sup>st</sup> Battery [ _BST ]	4Bh	Battery Remaining Capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 1E/1Fh. *7 *8
1 <sup>st</sup> Battery [ _BTP ]	4Ch	Battery Trip Point	R/(W)	DATA[23:16] *1 *7								-	0x00	PMU06A use this data with 22/23h. *7 *8
2 <sup>nd</sup> Battery [ _BIF ]	4Dh	Design capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 26/27h. *7 *8
	4Eh	Last Full Charge Capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 28/29h. *7 *8
2 <sup>nd</sup> Battery [ _BST ]	4Fh	Battery Remaing Capacity	R/(W)	DATA[23:16] *1 *7								-	0xff	PMU06A use this data with 42/43h. *7 *8
2 <sup>nd</sup> Battery [ _BTP ]	50h	Battery Trip Point	R/(W)	DATA[23:16] *1 *7								-	0x00	PMU06A use this data with 46/47h. *7 *8
	51h to 6Bh *3	Reserved	R/W	Don't care								-	-	

\*1: The register type is word.

\*2: Same as 1st Battery CMBatt Data

\*3: This register is not cleared if the system is in S4-S5 state.

R/(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	Default	Description
				7	6	5	4	3	2	1	0			
PMU Access	6Ch	PMU_LOW_ADR	R/W	DATA [7:0]								-	-	These registers are available when PMU slave mode or charger mode is selected. For detail information, refer to PMU slave communication section in this document
	6Dh	PMU_HIG_ADR	R/W	DATA [15:8]								-	-	
	6Eh	CHECK_SUM	R/W	DATA [7:0]								-	-	
	6Fh	PMU_DATA	R/W	DATA [7:0]								-	-	
SMBus	70h *7	SMB_PTCL	R/W	PROTOCOL[7:0]								-	-	For detail information, refer to ACPI 1.0 specification [ 13.9 SMBus Host controller Interface via Embedded controller]  These registers are not available when PMU slave mode or charger mode is selected.  The PMU06 has access protect function for the EEPROM in the battery, to cancel the protection, set the access protect cancel bit. For detail, refer to SMBus section
	71h *7	SMB_STS	R/W	D O N E	A L R M	R E S	STATUS [4:0]					-	-	
	72h	SMB_ADDR	R/W	ADDRESS [6:0]						R E S	-	-		
	73h	SMB_CMD	R/W	COMMAND								-	-	
	74h to 93h	SMB_DATA [0-31]	R/W	DATA								-	-	
	94h	SMB_BCNT	R/W	RES[7:5]			BCNT[4:0]					-	-	
	95h	SMB_ALARM_ADDR	R(W)	ADDRESS[6:0]						R E S	-	-		
	96h to 97h	AMB_ALARM_DATA[0-1]	R(W)	DATA								-	-	
	98h	SMB_CNRL	R/W	RES[7:1]						P R T	0x00	PRT =1 : The SMBus address (A8-AE) protection is cancelled.		
Reserved	99h to 9Fh	Reserved	R/W	Don't care								-	-	

\*7: When this register is checked by polling, the interval time is necessary more than 500usec.

R(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

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Function	Address	Register Name	R/W	Bit Number								Logic	De-fault	Description						
				7	6	5	4	3	2	1	0									
Status	A0h*3	ADP_STS	R/(W)	RES[7:1]							C O N	-	-	CON = 1 : AC adapter is connected						
	A1h*3	BAT1_STS (1st Battery)	R/(W)	B T P	E M P	L O W	W A R	E R R	D C H G	C H G	C O N	-	-	BTP =1: Battery trip point is detected. EMP =1: Battery is empty. LOW =1: Battery is Low battery WAR =1: Battery is warning state. ERR =1: Battery is Warning state. DCHG=1: Battery is Error state. CHG=1: Battery is discharged. CON=1: Battery is charged. Battery is connected.						
	A2h*3	BAT2_STS (2nd Battery)	R/(W)									-	-							
	A3h*3	Reserved	R/W	Don't care							-	-								
	A4h*3	BAT1_CAP	R/(W)	BCAP							-	-	0x00-0x64 = 0-100(%) 0x7F = Unknown 0x80 = Not installed							
	A5h*3	BAT2_CAP	R/(W)	BCAP							-	-								
	A6h*3	Reserved	R/W	Don't care							-	-								
	A7h	SMB_Alert_ADDR	R/W	ADDRESS[6:0]							R E S	-	0x00	SMBAlert output device address The alert response function is available when this register is cleared (0x00) only. When the several devices assert the alert signal at the same time, the least address is stored to this register. And when this register is cleared , next alert address is stored to this register.						
	A8h*5	GPIO-A_EVT_STS	R/W	STS_A [7:0]							Read 0:No event 1:EVT detection Write 0:Clear event 1:Ignore	0x00	To clear the notified event flag without unexpected event loss, clear the corresponding bit flag only. For this operation, this register has special writing manner as follows. STS_X <b>B</b> (STS_X) AND (Written data)							
	A9h*5	GPIO-B_EVT_STS	R/W	0	STS_B [6:0]							0x00								
	AAh*5	GPIO-C_EVT_STS	R/W	0	0	0	0	0	0	STS_C [1:0]		0x00								
	ABh*5	RUN_EVT_STS	R/W	B T P 2	S M B	A L R T	G P I O	R E S	B A T 2	B A T 1		A D P		0x00						
	ACH*5	WAKE_EVT_STS	R/W								0x00									
	ADh*5	RUN_EVT_STS_2	R/W								Reserved [7:1]							T H	0x00	
	A Eh*5	WAKE_EVT_STS_2	R/W								Reserved [7:1]							T H	0x00	
	AFh*5	THERMAL_EVT_STS	R/W	Reserved [7:3]							E R R L O W H I G H	0x00		STS_X <b>B</b> (STS_X) AND (Written data)						

\*3: This register is not cleared if the system is in S4-S5 state.

\*5: After writing to this register, Set the "00h" to the BURST\_FLG\_CLR register.

# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	De- fault	Description								
				7	6	5	4	3	2	1	0											
Event/ GPIO Control	B0h	EC_RUN_ENB	R/W	B T P 2	S M B	A L R T	RES[4:1]				A D P	0: Disable 1: Enable	0x00	BTP2: SMB : ALRT: ADP:	BTP2 event SMBus event. SMBAlert event. Adapter event.							
	B1h	EC_WAKE_ENB	R/W									0: Disable 1: Enable	0x00									
	B2h	BATT_RUN_ENB	R/W	B T P	E M P	L O W	W A R	E R R	C A P	C / D	C O N	0: Disable 1: Enable	0x00	BTP: EMP: LOW: WAR: ERR: CAP: C/D: CON:	Battery trip point Empty. Low battery Warning Error Capacity learning Charge/Discharge Battery presence							
	B3h	BATT_WAKE_ENB	R/W									0: Disable 1: Enable	0x00									
	B4h	GPIO-A_IO_CONF	R/W	CONF_A [7:0]								0: Input 1: Output	0x00	For detail information, refer to GPIO section in this document.								
	B5h	GPIO-A_DATA	R/W	DATA_A [7:0]									-									
	B6h	GPIO-A_RUN_ENB	R/W	RUN_ENB_A [7:0]								0: Disable 1: Enable	0x00									
	B7h	GPIO-A_EVT_POL	R/W	POL_A [7:0]								0: Falling edge 1: Rising edge	0x00									
	B8h	GPIO-A_WAKE_ENB	R/W	WAKE_ENB_A [7:0]								0: Disable 1: Enable	0x00									
	B9h	GPIO-B_IO_CONF	R/W	1								CONF_B [6:0]							0: Input 1: Output	0x80		
	BAh	GPIO-B_DATA	R/W	0								DATA_B [6:0]								-		
	BBh	GPIO-B_RUN_ENB	R/W	0								RUN_ENB_B [6:0]							0: Disable 1: Enable	0x00		
	BCh	GPIO-B_EVT_POL	R/W	0								POL_B [6:0]							0: Falling edge 1: Rising edge	0x00		
	BDh	GPIO-B_WAKE_ENB	R/W	0								WAKE_ENB_B [6:0]							0: Disable 1: Enable	0x00		
	BEh	GPIO-C_DATA	R/W	RES [7 :4] *4								DATA_C [3:0]					-					
	BFh	GPIO-C_RUN_ENB	R/W	0								0	0	0	0	0	0	RUN_ENB_C [1:0]	0: Disable 1: Enable	0x00		

\*4: Should be 0.



# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	De- fault	Description					
				7	6	5	4	3	2	1	0								
Event/ GPIO Control	C0h	GPIO-C_ EVT_POL	R/W	0	0	0	0	0	0	POL_ C [1:0]	0: Falling edge 1: Rising edge	0x00							
	C1h	GPIO-C_ WAKE_ENB	R/W	0	0	0	0	0	0	WAK E_ ENB _C [1:0]	0: Disable 1: Enable	0x00							
	C2h	EVT_CONT	R/W	RES [7:6]		WAK E		SCI *4		RES *4		Q_RU N		WAK E_ ENB _C [1:0]		SUS _X		0x00  WAKE SCI  Q_RU N  WAKE _OUT  SUS_X  =0: Wake# output is “Level”. =1: Wake# output is “Pulse”. =0: SCI is always output by event detection and SCI_EVT shows the query data is stored. And next SCI is not output until SCI_EVT is cleared. =1: SCI is output when the command set is not executed and OBF=0. SCI_EVT shows the output SCI is for event notification. =0: Runtime event ststus is reflected to RUN_EVT_STS register. =1: Runtime event status is reflected to Query data. =0: Wake event output is always enable.( in S0-S3) =1: Wake event output is enable when SUS_X=L. =0: Runtime and Wakeup is selected by SUS_B. (GPIO B6 is enable) =1: Runtime and Wakeup is selected by SUS_A. (GPIO B6 is used as SUS_A input.)	
	C3h	EC_RUN_ ENB_2	R/W	Reserved [7:1]						TH		0: Disable 1: Enable		0x00	TH: Thermal event				
	C4h	EC_WAKE_ ENB_2	R/W									0: Disable 1: Enable		0x00					
	C5h To C7h	Reserved	R/W	Don’ t care						-		-							
	C8h *6	GPI_AD0	R	AD0_DATA [7:0]						-		-	For detail information, refer to GPIO section in this document.						
	C9h *6	GPI_AD1	R	AD1_DATA [7:0]						-		-							
	CAh *6	Reserved	R/W	Don’t care						-		-							
	CBh	D/A_CONT	R/W	DATA [7:0]						-		0xff	0x00-0xfe: D/A converter output data 0xff : Battery capacity(%) output						
CCh	WAKE_DIS	R/W	DATA [7:0]						-		0x00	0x00 : WAKE# output enable 0x01 : WAKE# output disable							

\*4: Should be 0.

\*6: This register's response time is 150usec max.

# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	De-fault	Description
				7	6	5	4	3	2	1	0			
Battery control	D0h	BAT_CHG_CONT	R/W	RES[7:5]			CHG RDY#	RES[3:2]		CHG 2	CHG 1	-	-	CHG_RDY# =0 : Charge ready CHGn =1 : The nth battery is charged
	D1h	BAT_DCH_PRI	R/W	RES[7:3]				PAT [2:0]				-	0x00	Battery discharge priority 0 : 2 1 1 : 1 2 2 : 2 1 3 : 2 1 4 : 1 2 5 : 1 2 6 : Same as 0 7 : Simultaneously discharge (Read only :This data can be set using PMU register)
	D2h	BAT_DCH_CONT	R/W	RES[7:2]						DCH 2	DCH 1	0: Not discharge 1: Discharge	-	The discharge battery can be selected one of the batteries can be discharged.
	D3h	BAT_WAR_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Warning detection point 0x0000-0xffff (mWh)
	D5h	BAT_LOW_ABS	R/W	DATA[15:0] *1								-	0x0000	Absolute capacity battery Low detection point 0x0000-0xffff (mWh)
	D7h	BAT_WAR_REL	R/W	DATA [7:0]								-	0x10	Relative capacity battery Warning detection point 00-C8h (0-100% step 0.5%)
	D8h	BAT_LOW_REL	R/W	DATA [7:0]								-	0x06	Relative capacity battery Low detection point 00-C8h (0-100% step 0.5%)
	D9h *3	FULL_DATA	R/W	DATA [7:0]								-	0xbe	Full charge cancel point 00-C8h (0-100% step 0.5%)
	Dah	CC_CUR_DATA	R	DATA [7:0]								-	0x00	Battery charging current setting 0x01-0xff (0.02-5.10A step 0.02A) 0x00 Depends on the battery This register is "read only", to change the value, use the register in PMU registers area.
	DBh To DCh	BTP2	R/W	DATA [15:0]								-	0x0000	0x0000: Clear the trip point 0x0001-0xffff : (mWh) When all of the battery's capacities lesser than this setting value, the BTP2 is detected if event is enabled.
	DDh To DFh	Reserved	R/W	Don't care								-	-	

\*3: This register is not cleared if the system is in S4-S5 state.

R(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

# Software Functional Overview

Function	Address	Register Name	R/W	Bit Number								Logic	De-fault	Description
				7	6	5	4	3	2	1	0			
PMU control	E0h	PMU_CONT	R/W	RES[7:3]					EC - REG	BAY - LED	POW - LED	-	0x00	EC_REG = 1: PMU does not initialize E register when system power is off. BAY_LED = 1: PMU indicates the Battery discharge status to the LED_BAY#n, when the battery is installed. POW_LED = 1: The Power LED blink
	E1h	ACPI_ACC_ENB	R/W	RES [7:1]							OS - STS	-	0x00	OS_STS = 1: ACPI mode = 0: Legacy mode
	E2h	OFF_TIME	R/W	DATA [7:0]								-	0x64	Power switch over ride function timer 01h-FFh (0.1-25.5sec step 0.1sec) 00h : Reserved
Thermal Sensor Polling	E3h	POLLING_ADDRESS	R/W	Slave Address [6:0]							RES		0x00	Address: 0x00-0x7F The polling slave address setting If this address is 00, the Polling is disabled.
	E4h	HIGH_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data GE this value, the event will be detected.
	E5h	LOW_ALARM	R/W	DATA [7:0]								Signed value	0x00	If the received data LE this value, the event will be detected.
	E6h	POLLING_INTERVAL	R/W	DATA [7:0]									0x00	0x00 :Polling disable 0x01 – 0xFF [x 250ms] (250ms to 63.75sec)
	E7h	POLLING_DATA	R/(W)	DATA [7:0]								Signed value	0x00	This register shows data at latest polling.
	E8h	HARDWARE_SHUT_DOWN	R/W	DATA [7:0]								Signed value	0x7D	If the thermal sensor read value GE this value, the PMU automatically off the power.
	E9h	POLLING_COMMAND	R/W	DATA [7:0]									0x00	Polling command (data register) address.
	EAh	RETRY_COUNT	R/W	DATA [7:0]									0x10	0x00 - 0xFF: Retry count value (0-255)
	EBh To EFh	Reserved	R/W	Don't care										
PMU control	F0h	BURST_FLG_CLR	R/W	DATA [7:0]								-	-	After writing to the register addressed A8h-AFh, Set the 00h to this register.
	F1h To FFh	Reserved	R/W	Don't care										

R/(W): This is the read only register, but the written data will be able to read back till PMU updates the data periodically, or PMU detects the status change.

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## 3.9 Miscellaneous

### 3.9.1 Power Button

The system may have different action upon pressing the Power Button when the system is in the different state.

System Power State	Action for Pressing Power Button
Full-on	Power Off
Stand by	Power Off
STR	Resume from STR
STD	Resume from STD
SOff/MOff	Power On

### 3.9.2 Security

The user may enter up to 8 standard text characters for a password. The password includes two levels. The higher priority is the Supervisor Password. The lower priority is the User Password. The Supervisor Password can access all the system resource, while the User Password may not access the floppy disk when it is protected by Supervisor Password. Also, the User Password may not access the floppy disk when the Supervisor Password protects it.

When the security function is enabled, the system will request the user to enter password during the following situation:

- Power On → The system will prompt the user to enter the password before booting the OS. If the user key in the wrong password for 3 times, then the system will halt.
- Resume → The system will prompt the user to enter password while resuming from STR or STD mode. If the user keys in the wrong password for 3 times, the system will not resume and should return to Suspend mode.
- Entering CMOS Setup → The system will prompt the user to enter the password before entering the CMOS Setup. If the user keys in the wrong password for 3 times, then the system will halt.

## 3.10 CMOS Setup Utility

The Setup utility is used to configure the system. The Setup contains the information regarding the hardware for boot purpose. The changed settings will take effect after the system rebooted. Refer to Chapter 1 on running BIOS Setup Program for more detailed information.

## 3.11 Definitions of Terms

**10Base-T (Ethernet)** - A networking standard that supports data transfer rates up to 10Mbps (10 megabits per second).

**100Base-T (Fast Ethernet)** - A relatively new networking standard that supports data transfer rates up to 100Mbps.

**ACPI** - Advanced Configuration and Power Management Interface, a power management specification developed by Intel, Microsoft, and Toshiba.

**CardBus** - The 32-bit version of the PCMCIA PC Card standard. In addition to

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supporting a wider bus (32 bits instead of 16 bits), CardBus also supports bus mastering and operation speeds up to 33MHz.

**Clock Throttling** – South bridge function that allows the CPU clock to be stopped and started at a known duty cycle using the STPCLK# pin to enter and exit Stop Grant mode. Clock throttling is used for power saving, thermal management, and reducing the processing speed.

**DIMM (SODIMM)** - Dual In-line Memory Module, a small circuit board that holds memory chips. A Single In-line Memory Module (SIMM) has a 32-bit path to the memory chips whereas a DIMM has 64-bit path. Because the Pentium processor requires a 64-bit path to memory, you need to install SIMMs two at a time. With DIMMs, you can install one DIMM at a time. SODIMM is Small Outline Dual In-line Memory Module used in notebook computers.

**DMI** - Desktop Management Interface, an API to enable software to collect information about a computer environment about a computer environment. For example, using DMI a program can determine what hardware and expansion boards are installed on a computer.

**GPI** - General Purpose Input.

**GPO** - General Purpose Output.

**Lid Switch** - A switch that indicates the notebook LCD Panel has been closed and it can be turned off.

**MPEG-2** - Moving Picture Experts Group, a working group of ISO. The term also refers to the family of digital video compression standards developed by the group. There are two major MPEG standards : MPEG-1 and MPEG-2. The most common implementations of the MPEG-1 standard provide a video resolution 352x240 at 30 frames per second(fps). A newer standard, MPEG-2, offers resolution of 720x480 and 1280x720 at 60 fps, with full CD-quality audio.

**North Bridge** - The CPU to PCI interface, also contains the memory and cache controllers.

**South Bridge** - The PCI to ISA interface, also contains many legacy devices.

**SMM** - System Management Mode, Mode of operation while an SMI is active.

**SMI** - System Management Interrupt, non-maskable interrupt that causes the system to enter SMM. SMM functions include power management, USB legacy keyboard control, security, hot keys, and thermal monitoring.

**SMB** - System Management Bus, that is used for managing smart batteries, reading SDRAM configuration information, and other miscellaneous system function.

**TBD** -To Be Discussed. The mentioned specification is not final that should be discussed with related engineers.

**Ultra DMA-33** - A protocol developed by Quantum Corporation and Intel that supports burst mode data transfer rates of 33.3 MBps.

**USB** - A new external bus standard that supports data transfer rates of 12 MBps. A single USB port can be used to connect up to 127 peripheral devices, such as mice, modems, and keyboards. USB also supports Plug-and-Play installation and hot plugging.